

iSwitch: Accelerating Distributed Reinforcement Learning with In-Switch Computing

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Electrical & Computer Engineering

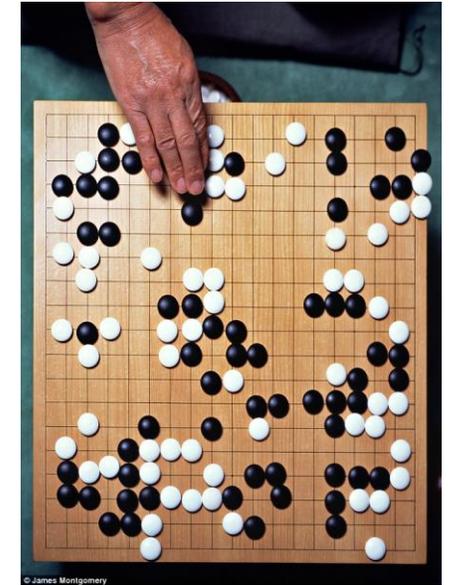
AI Applications are Increasingly Operating in Dynamic Environments



Autonomous Driving



Robotics



Games

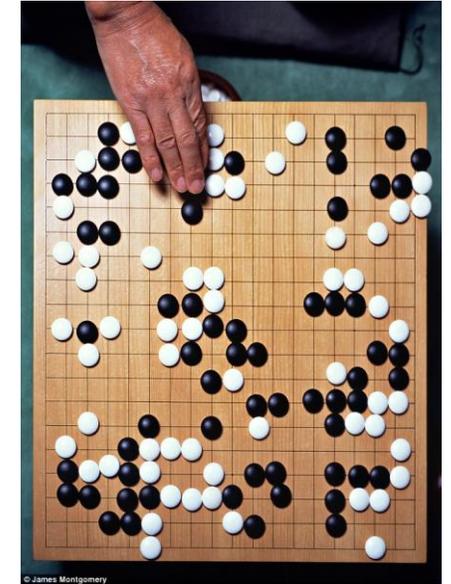
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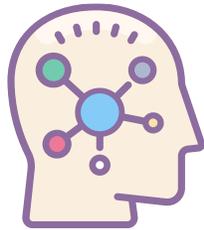
Robotics



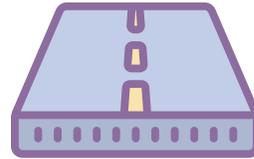
Games

Reinforcement Learning Empowers AI Applications to Take Real-Time Intelligent Actions

What is Reinforcement Learning?



Agent

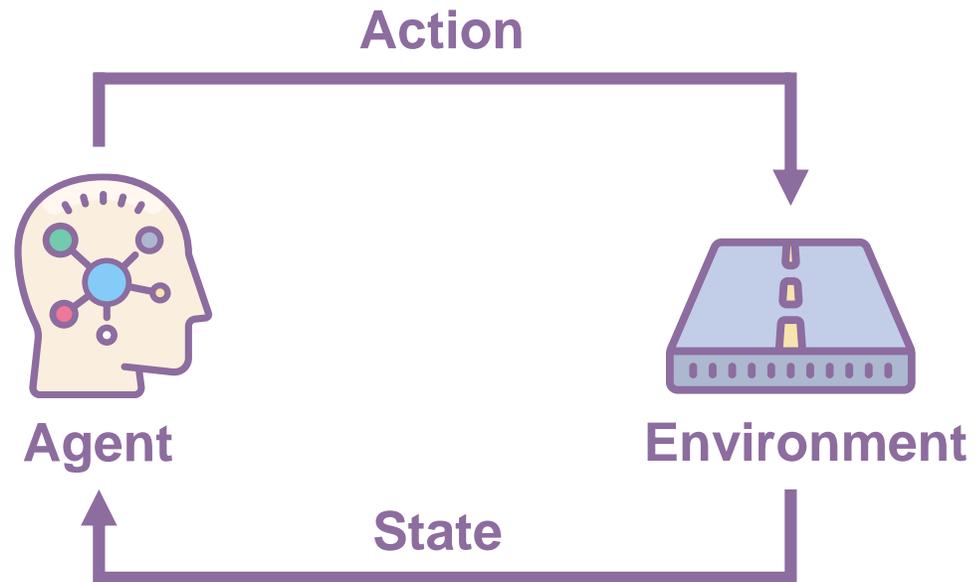


Environment

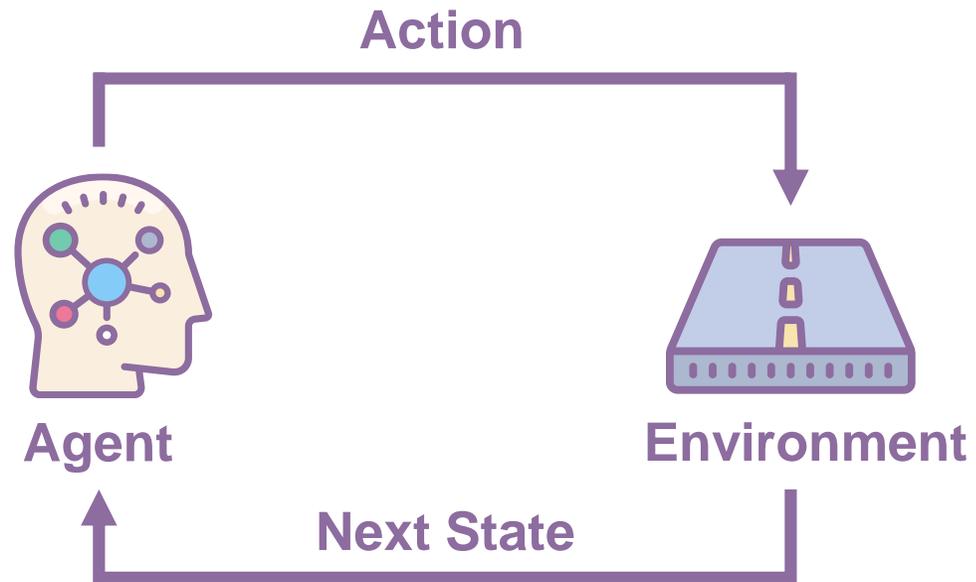
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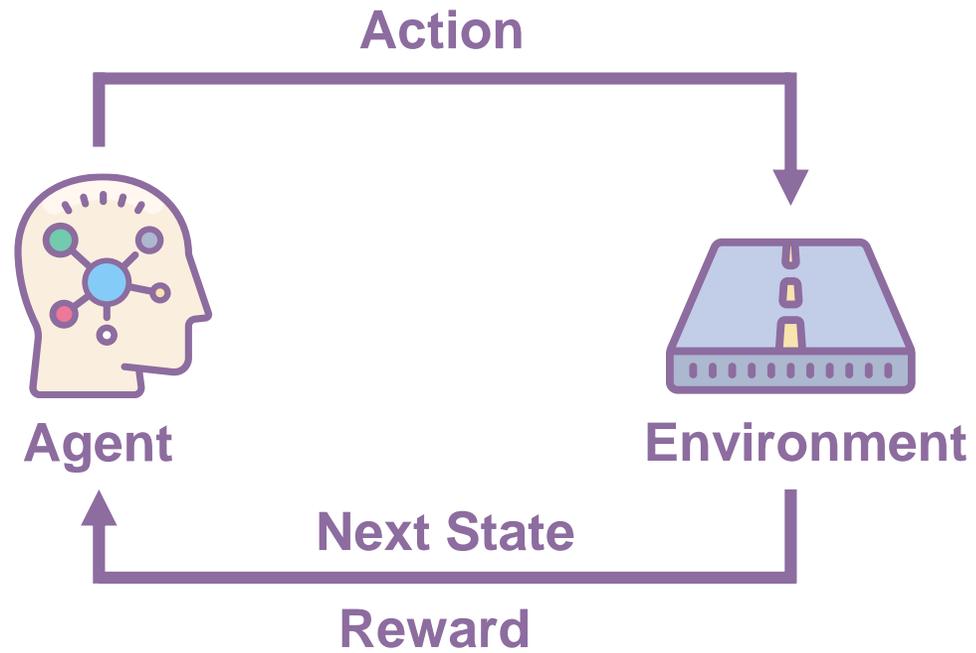
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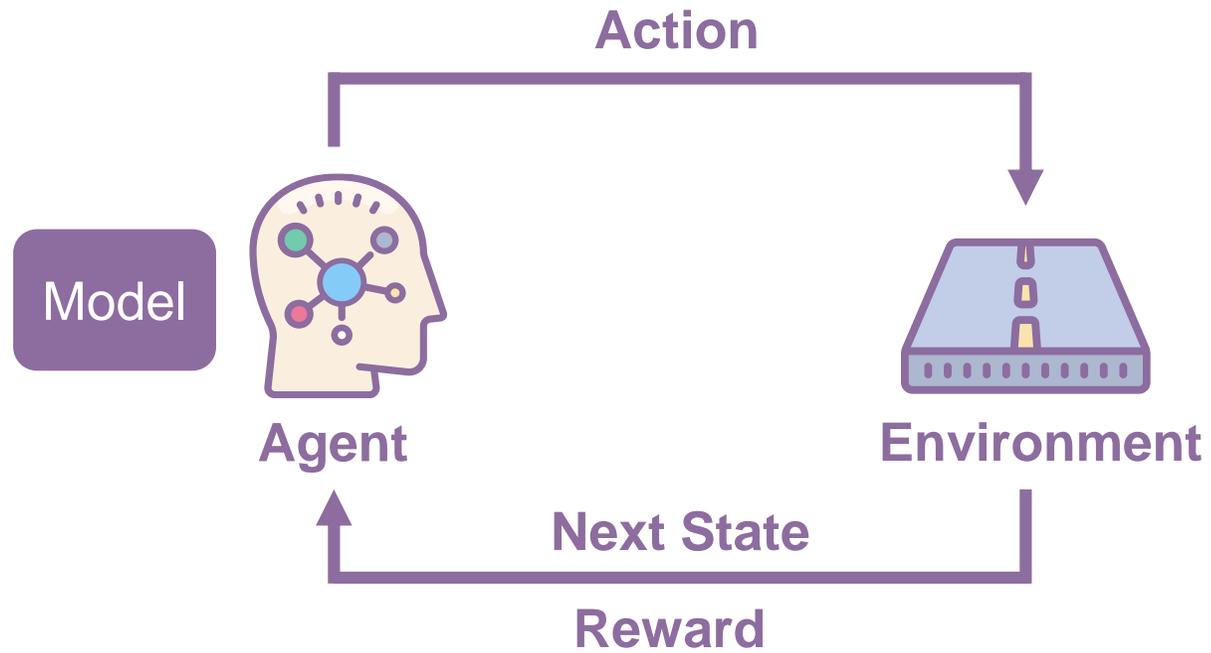
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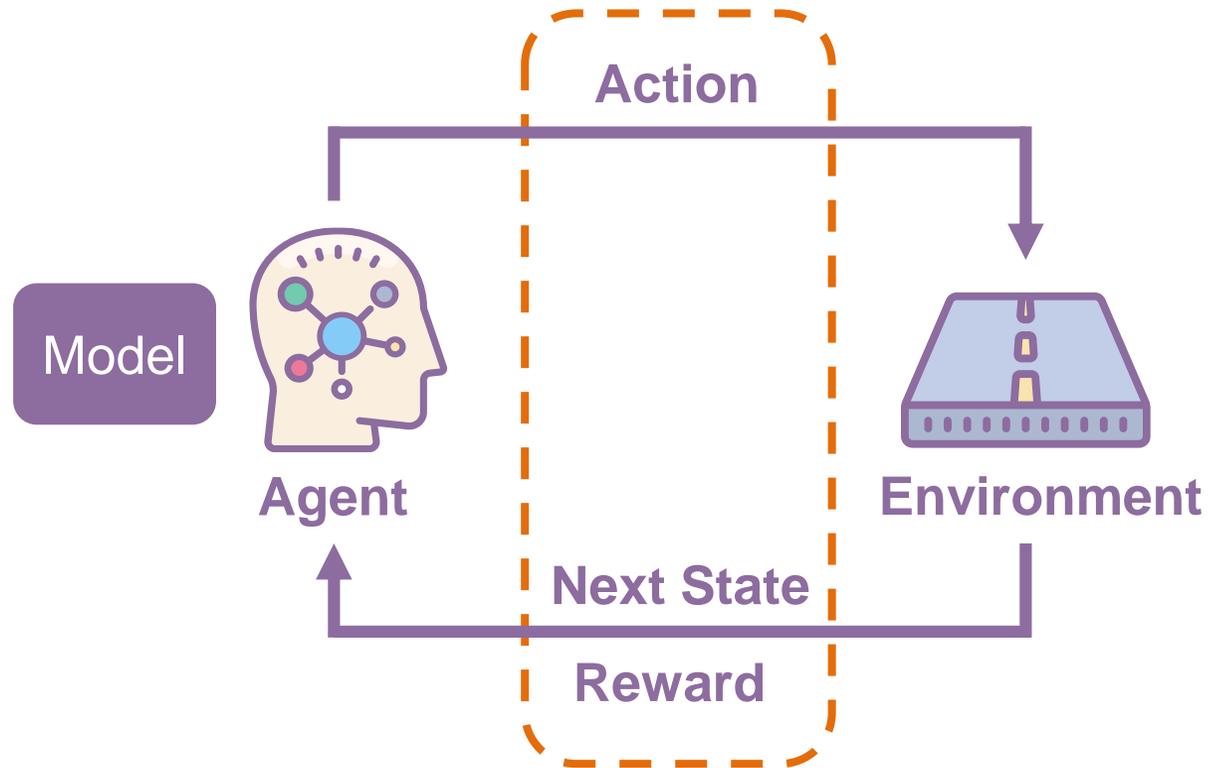
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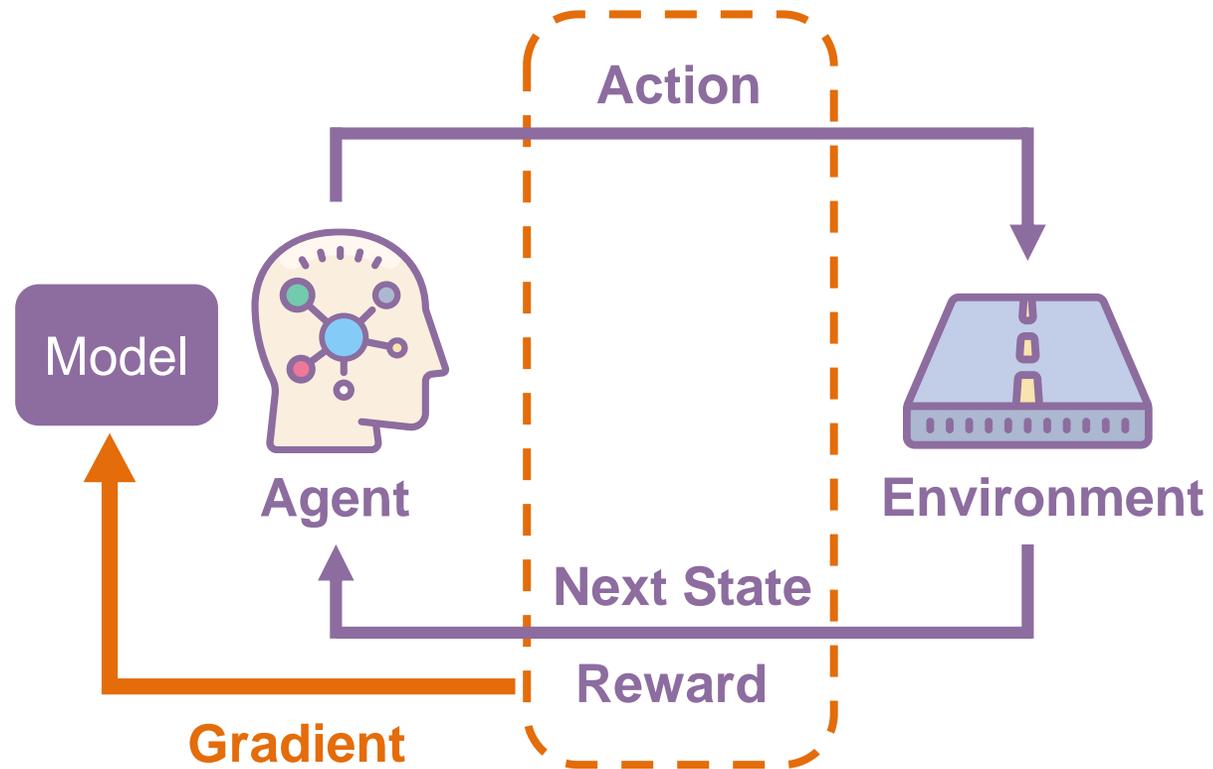
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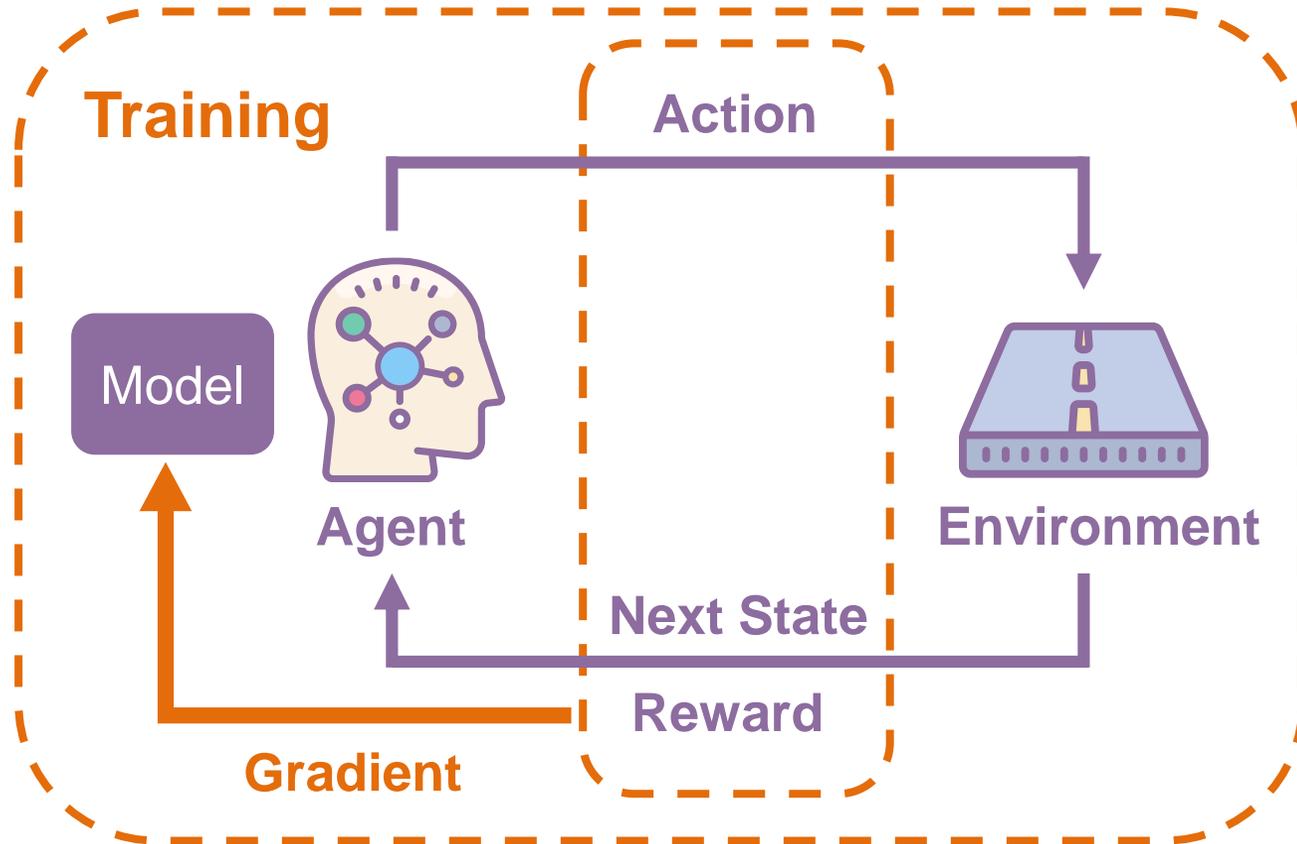
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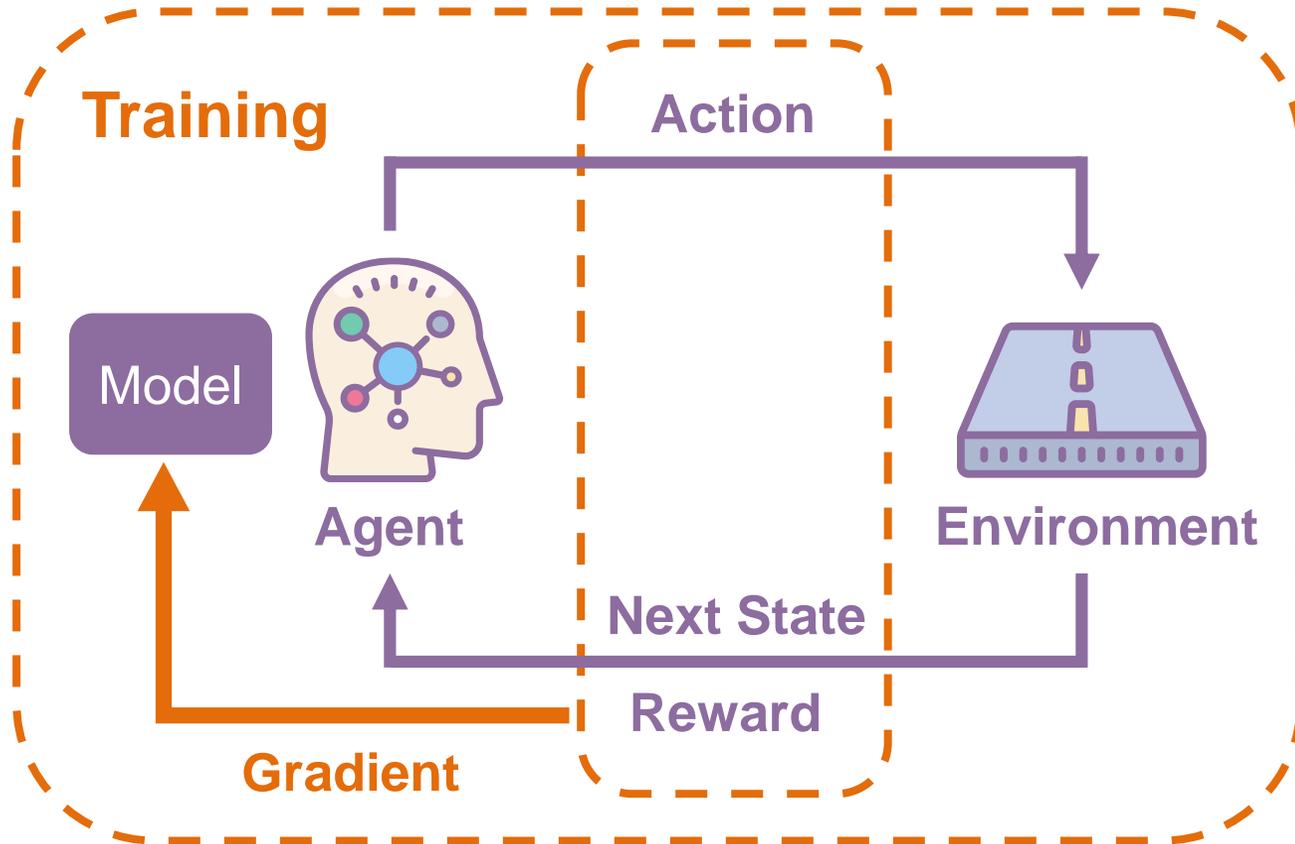
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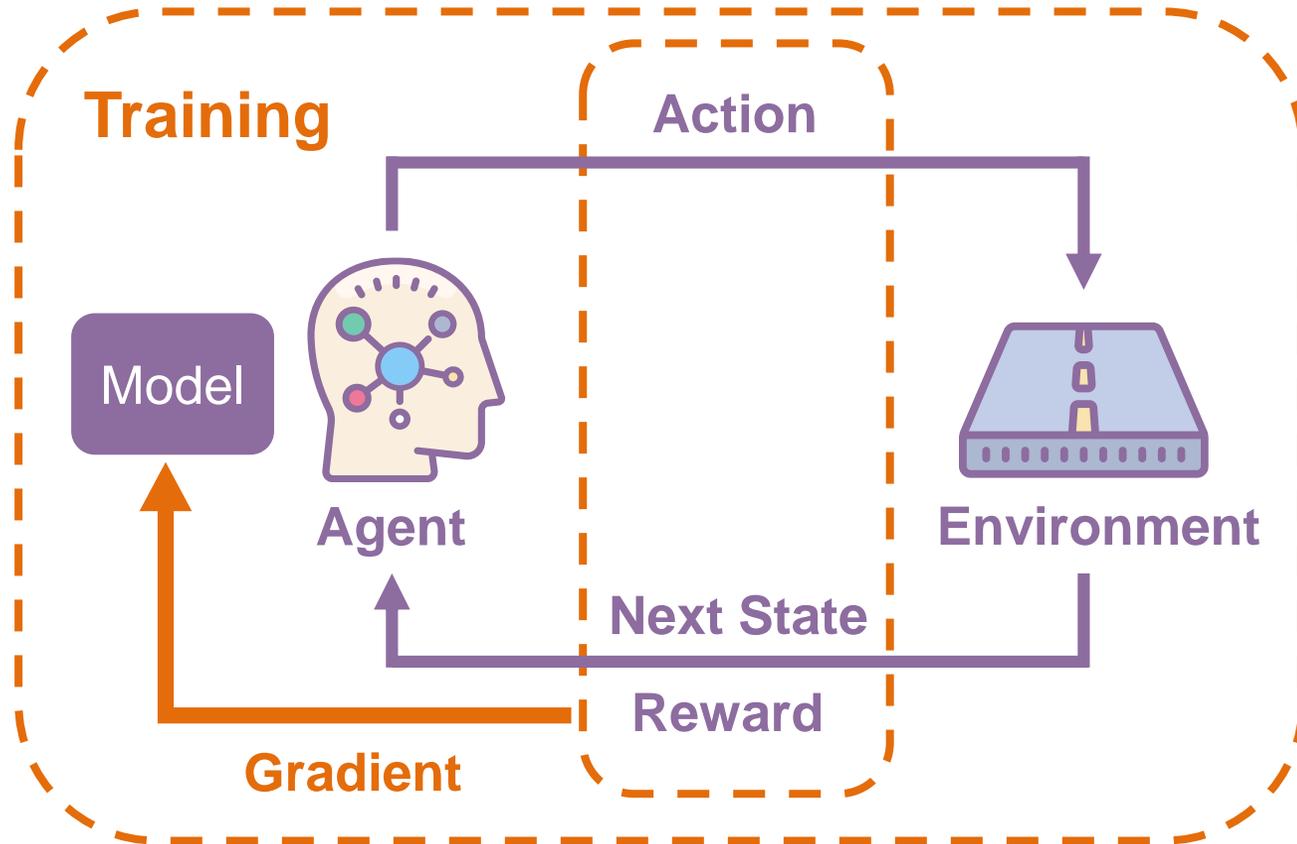


Train a Typical RL Agent on a Single GPU = 8 Days*



*Mnih, ICML'16

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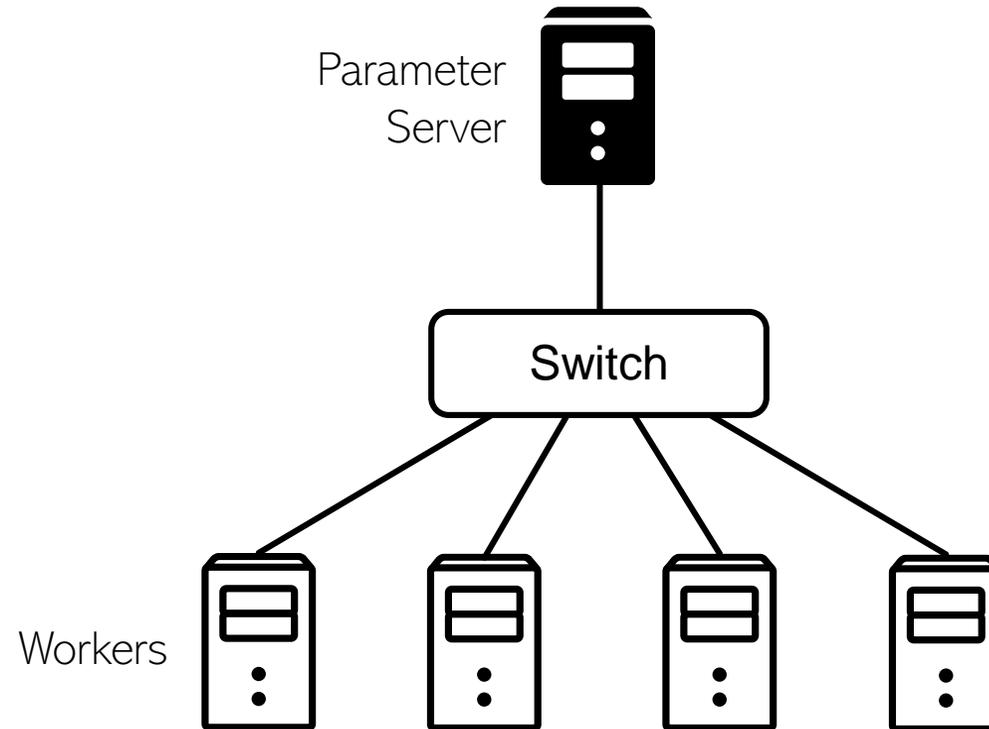
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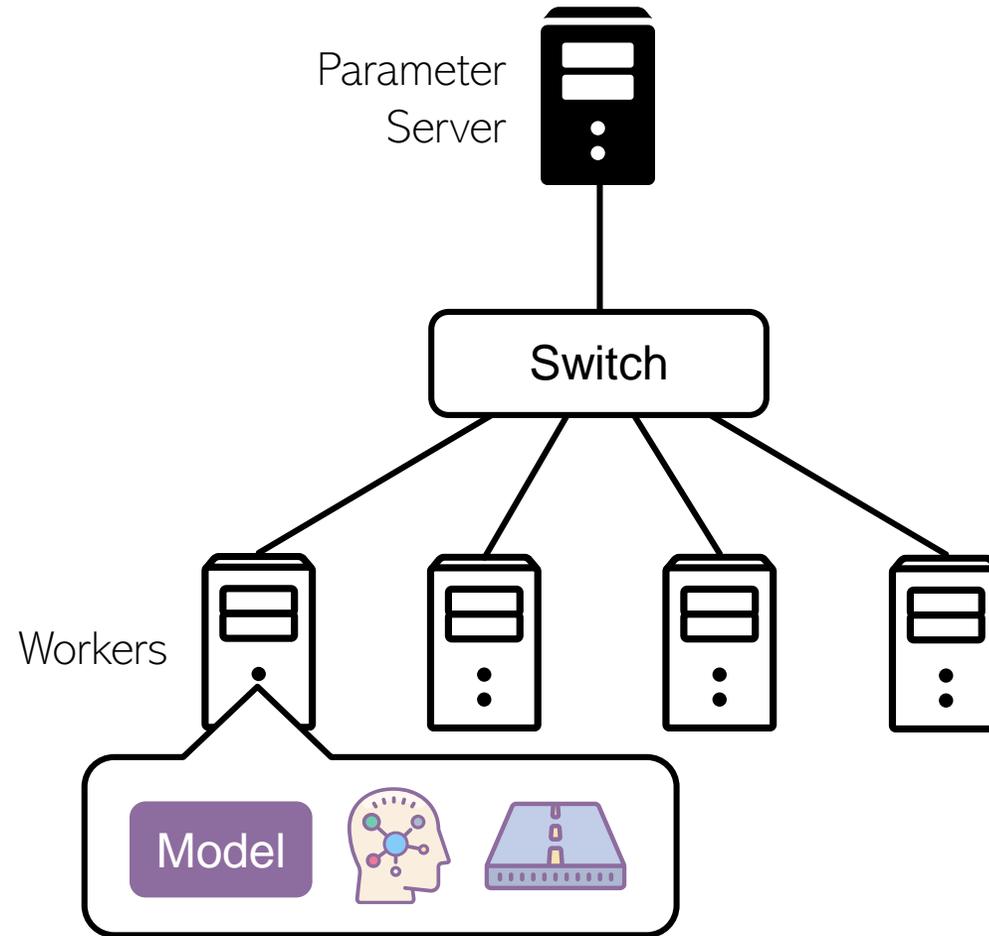
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RL Requires Distributed Training for Improved Performance

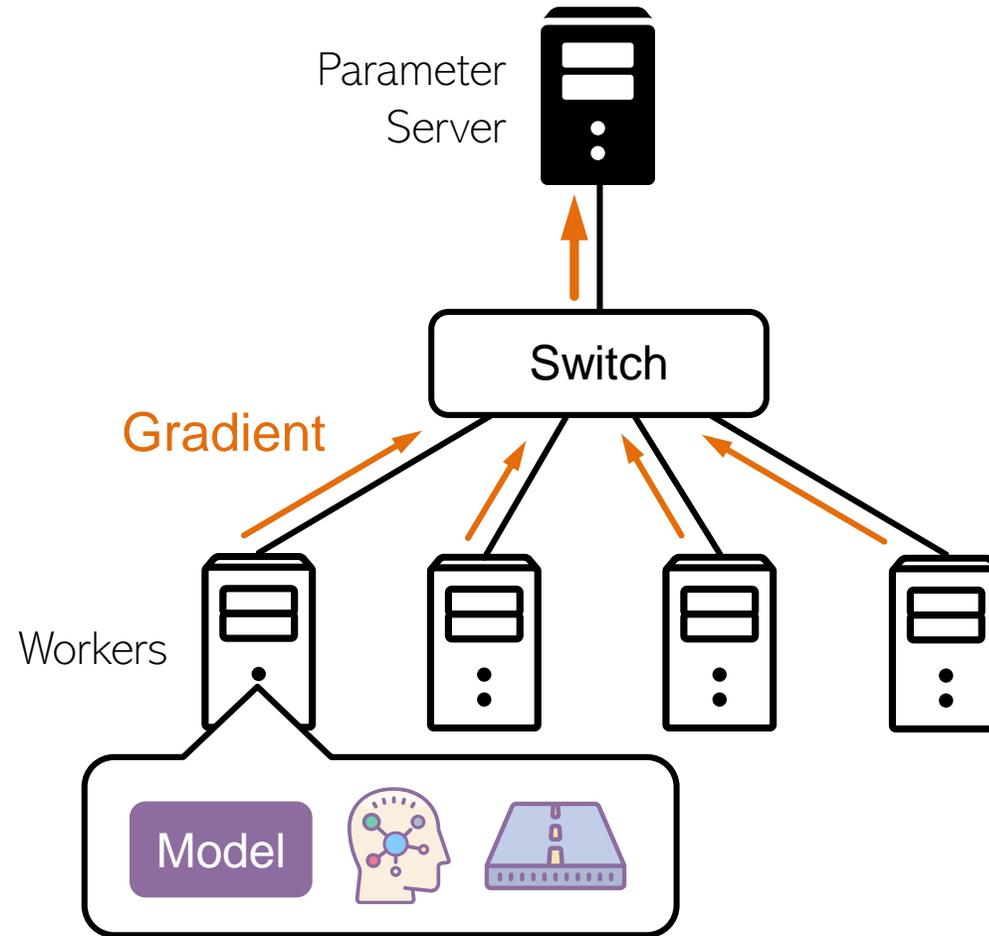
Centralized Distributed RL Training: Parameter-Server Based



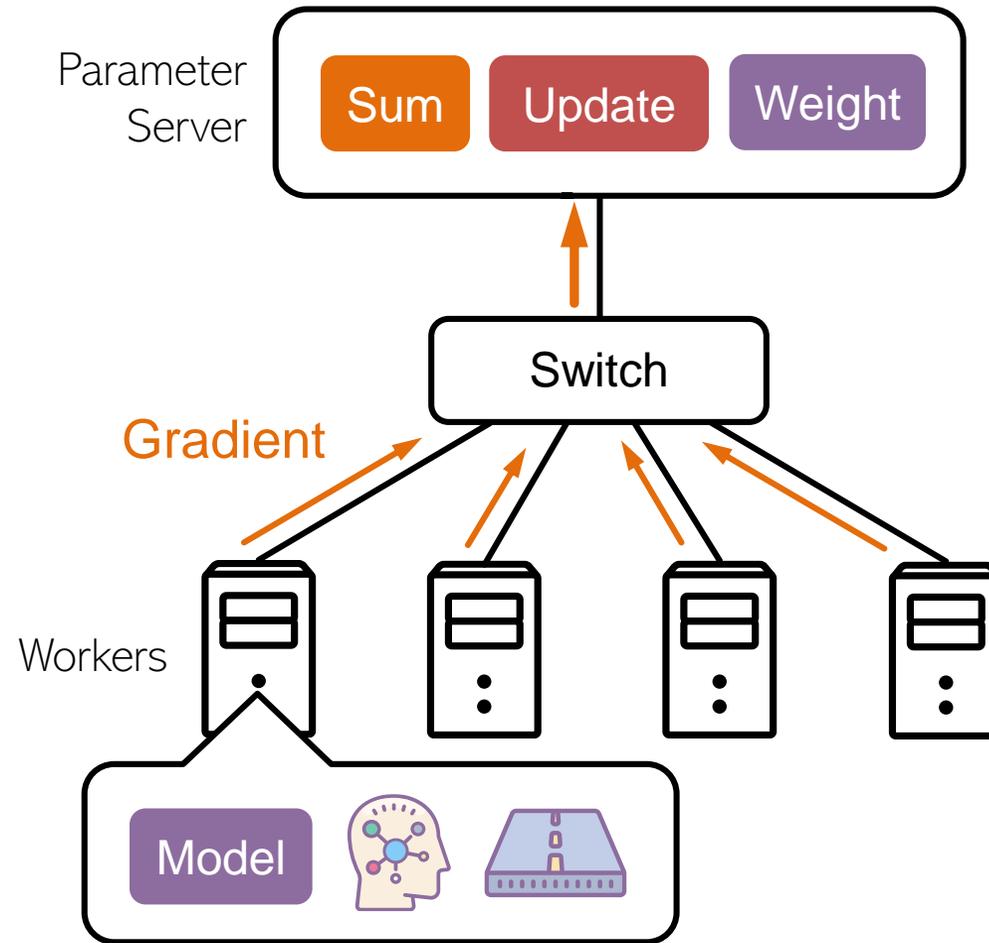
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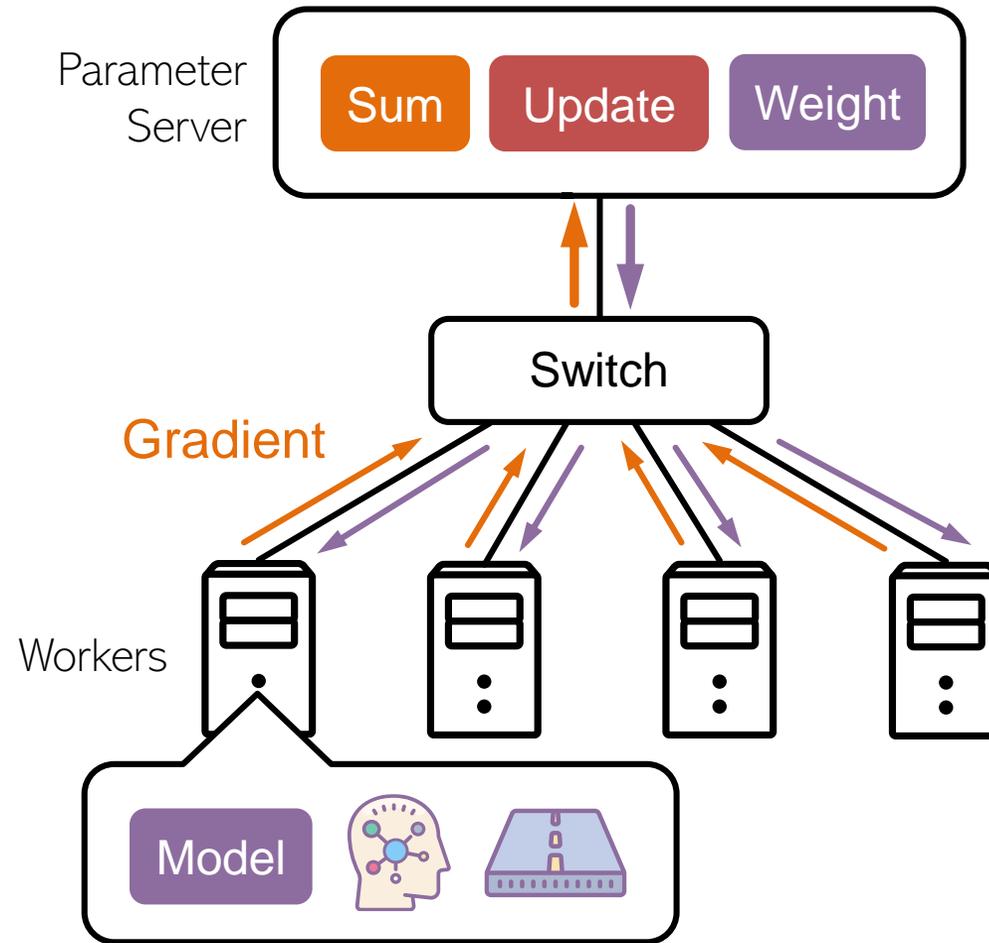
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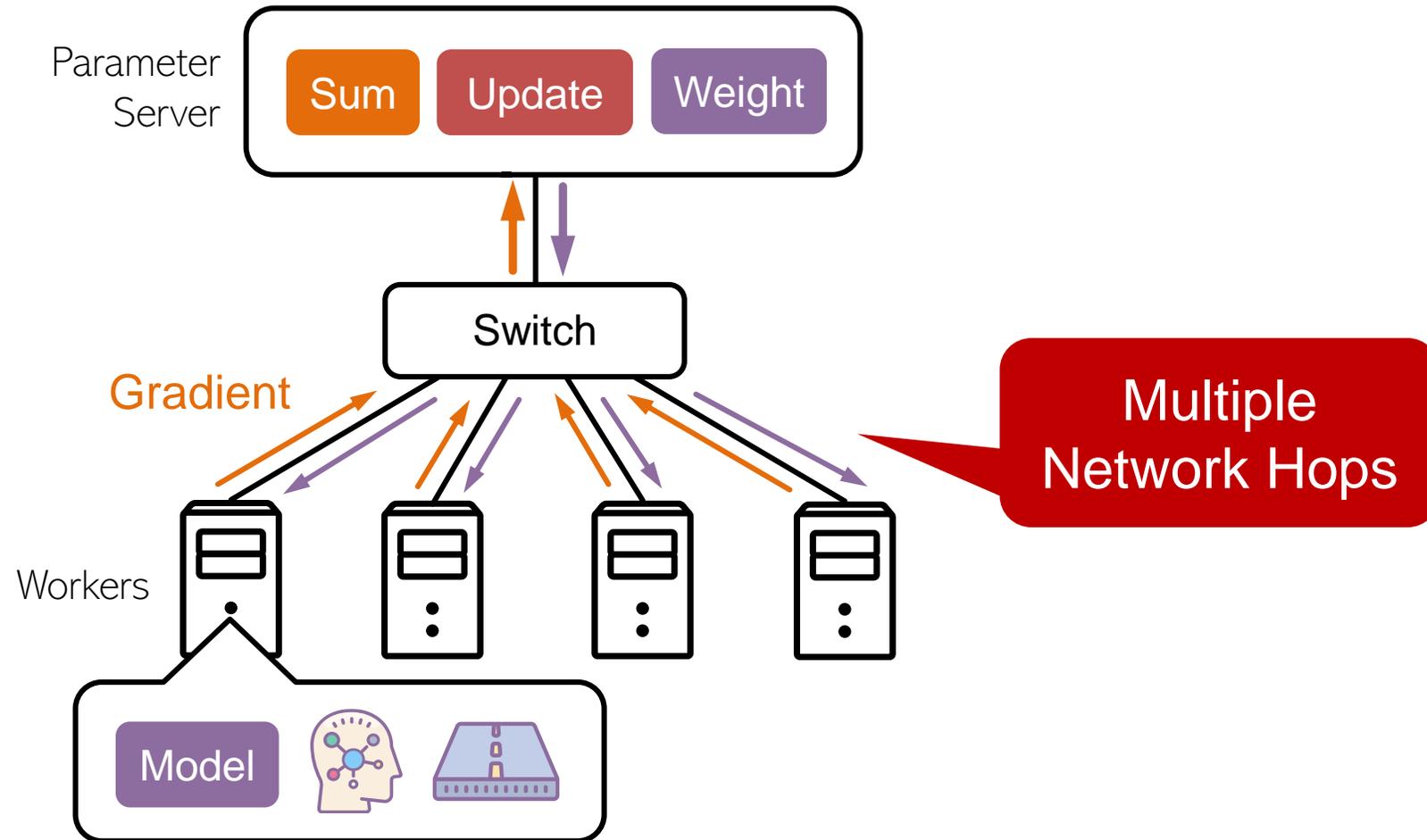
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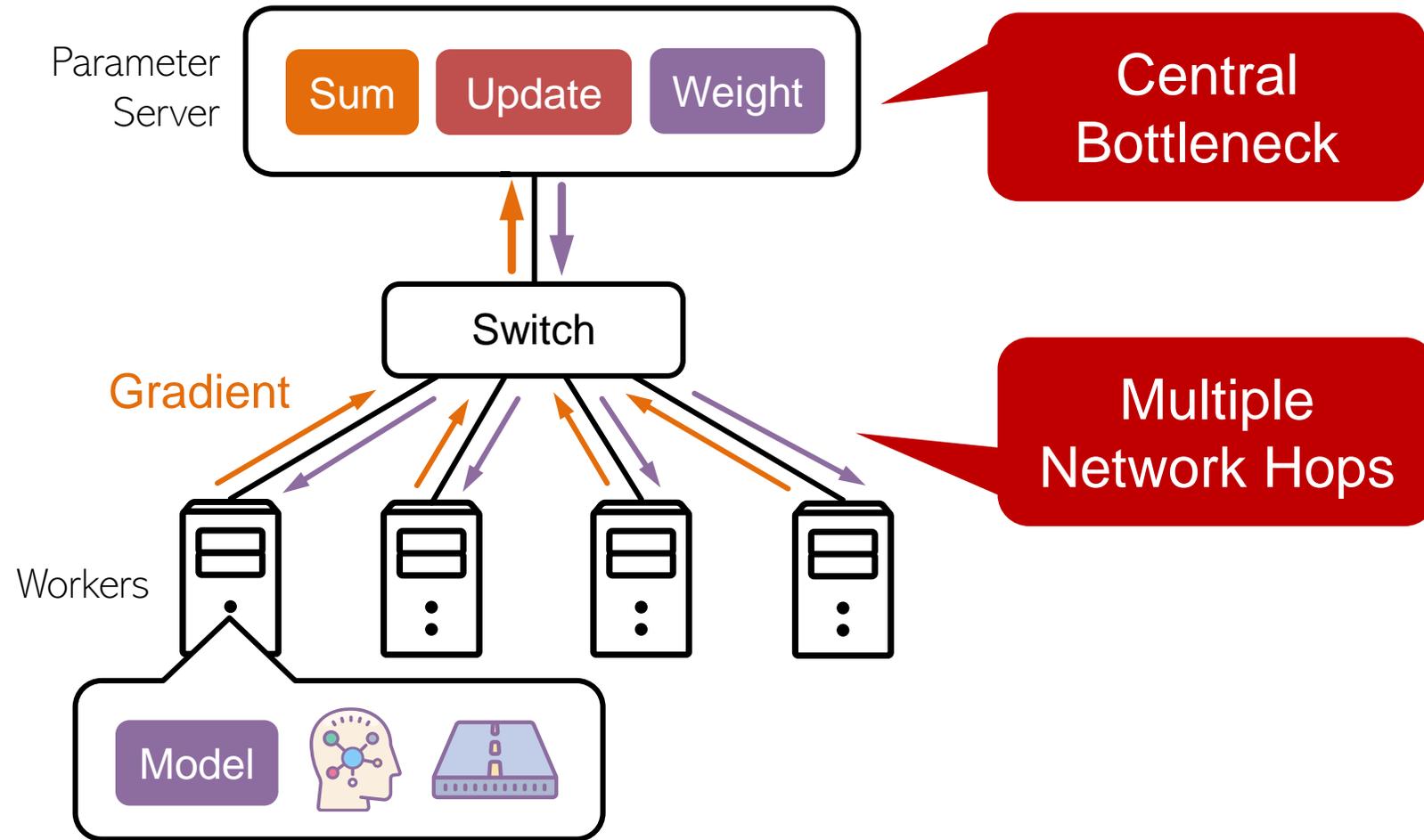
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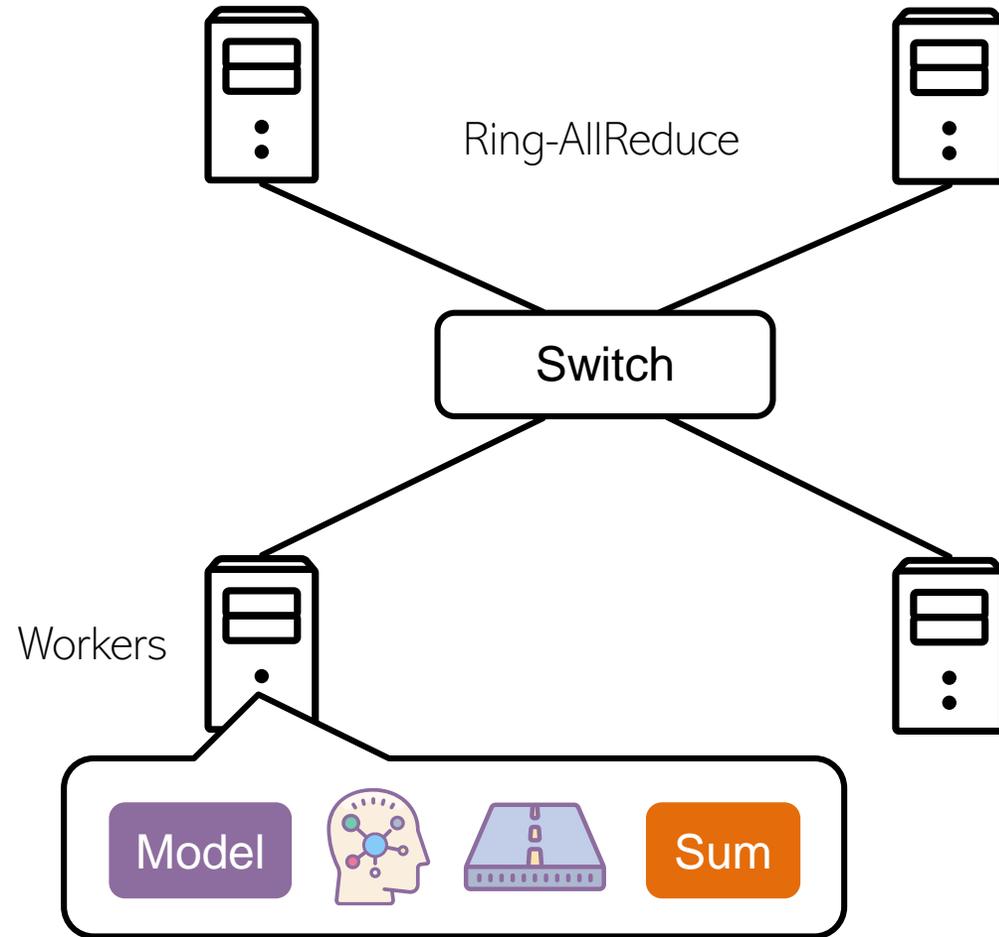
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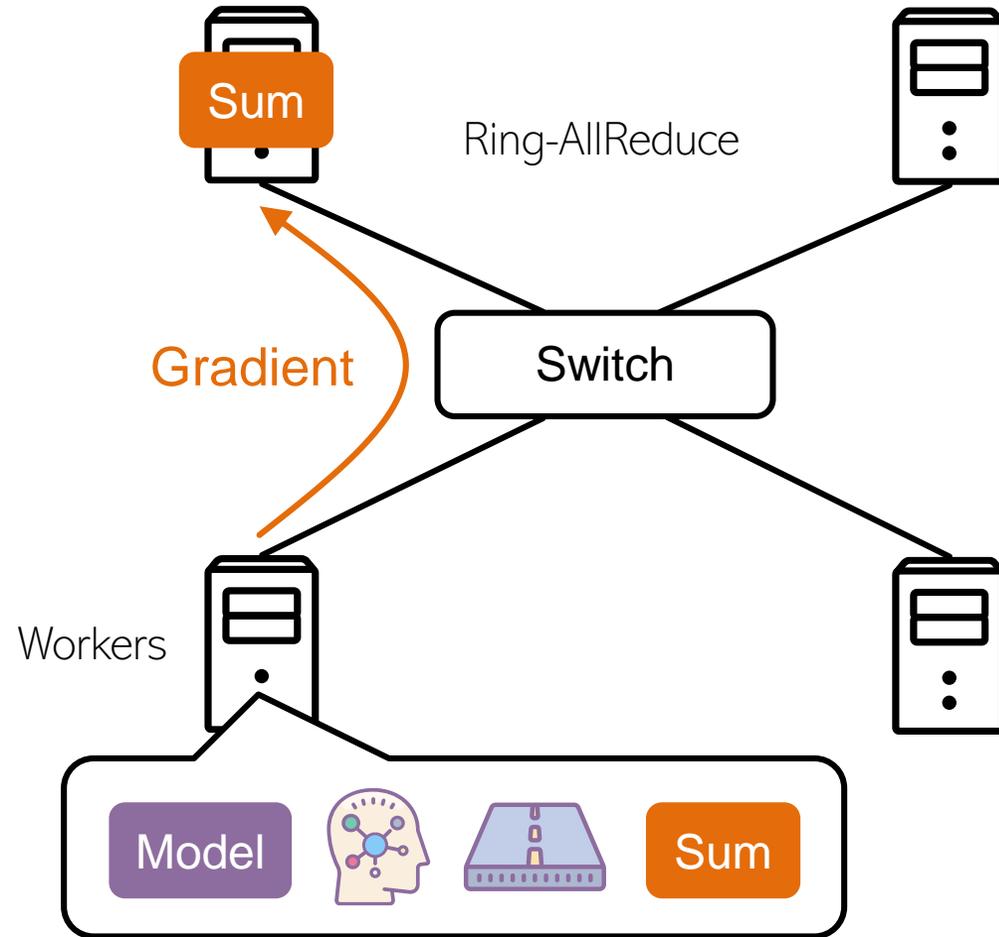
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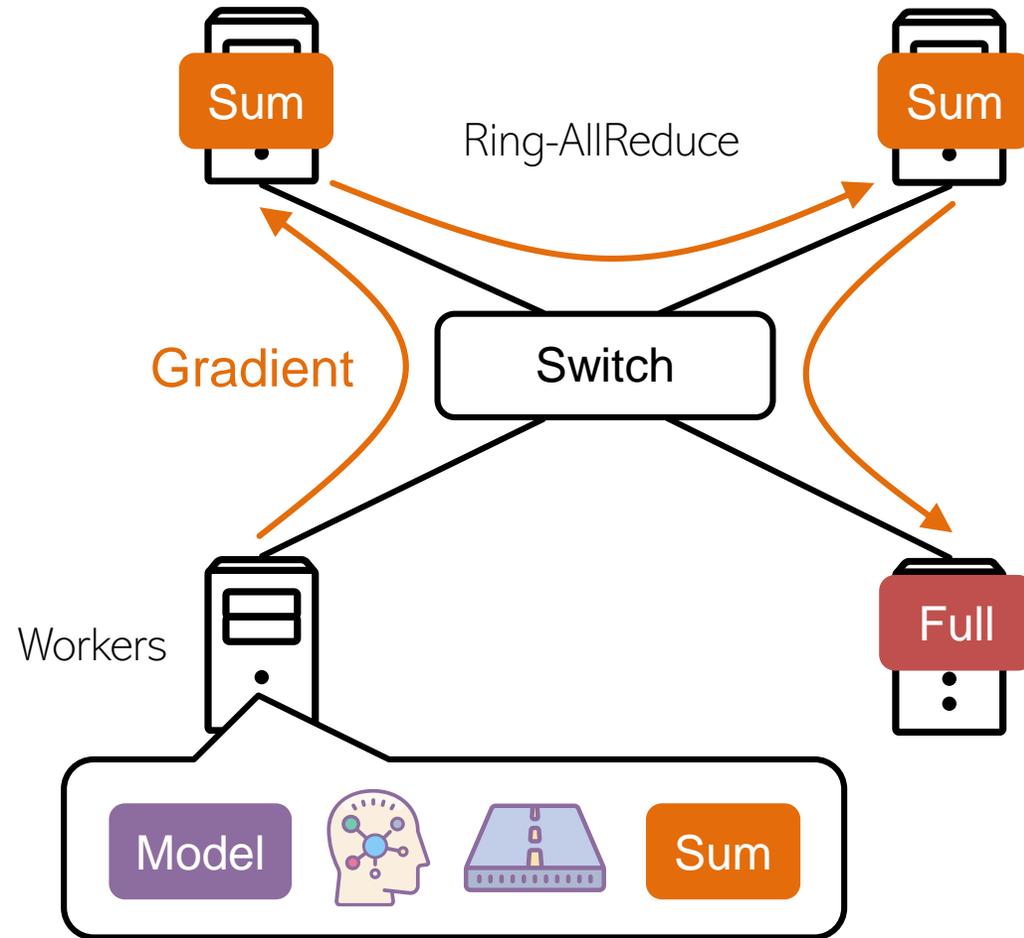
Decentralized Distributed RL Training: AllReduce Based



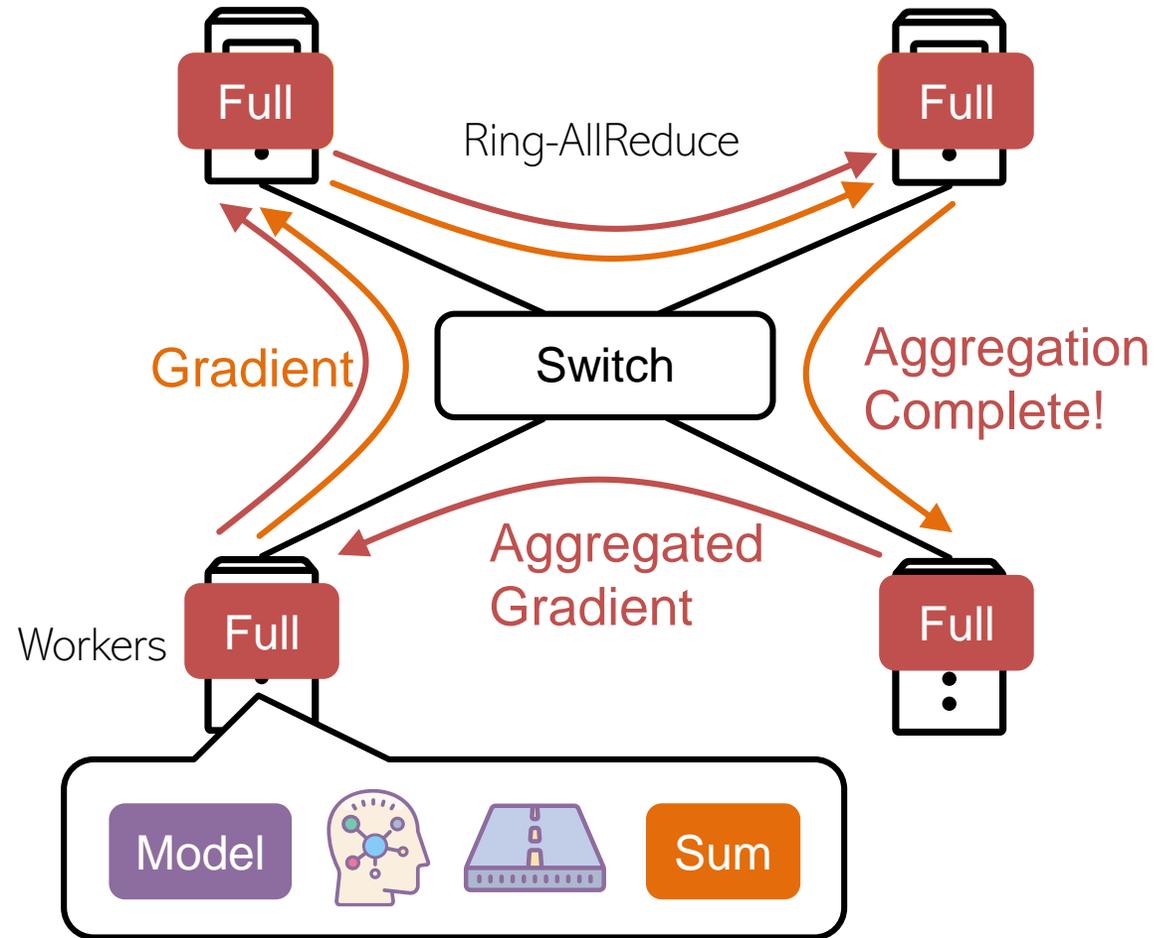
Decentralized Distributed RL Training: AllReduce Based



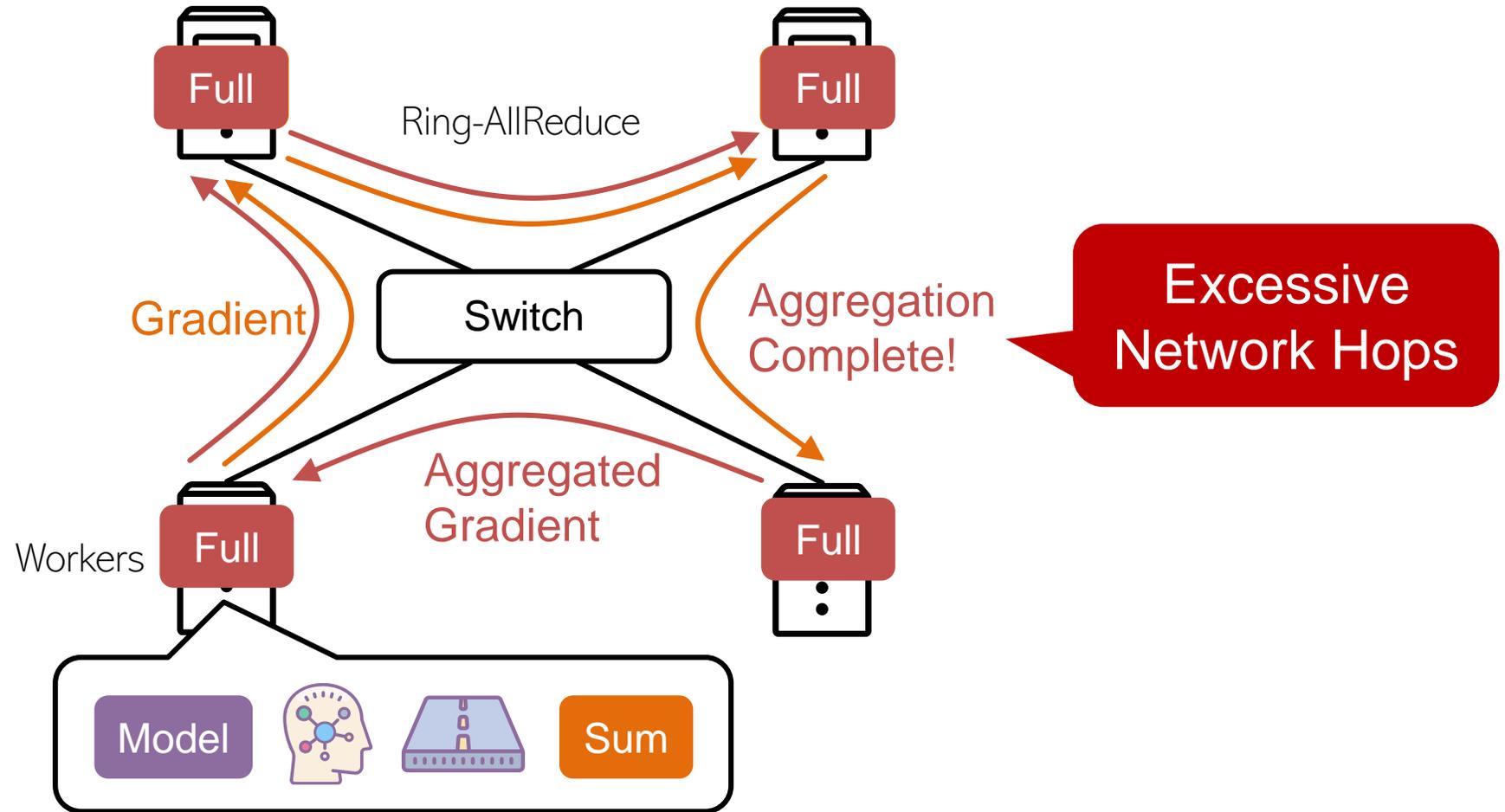
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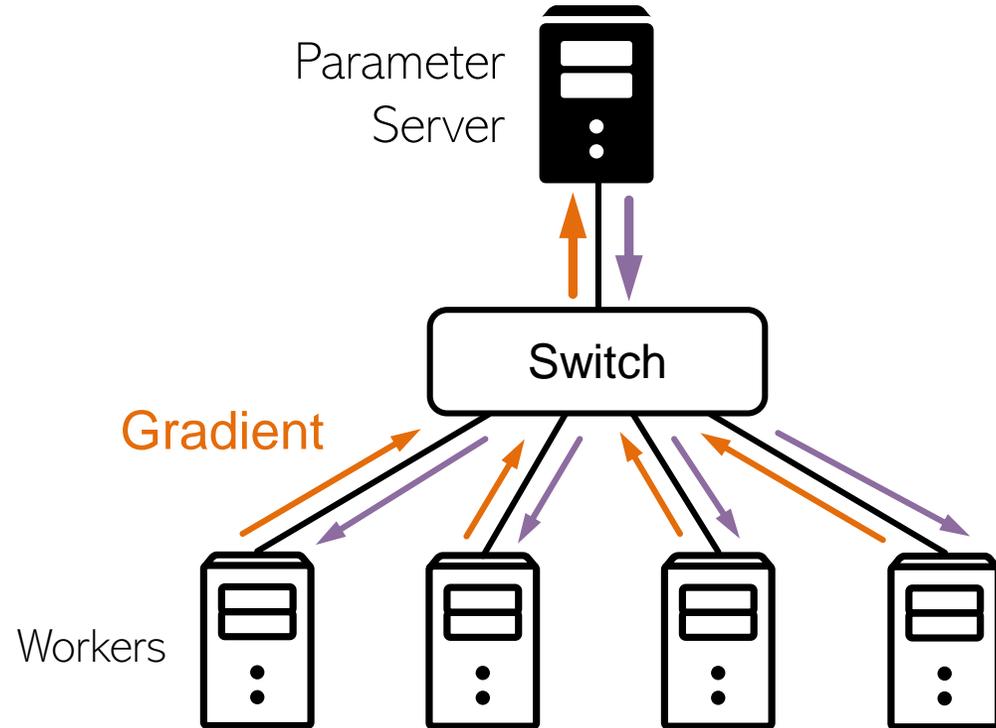


Decentralized Distributed RL Training: AllReduce Based

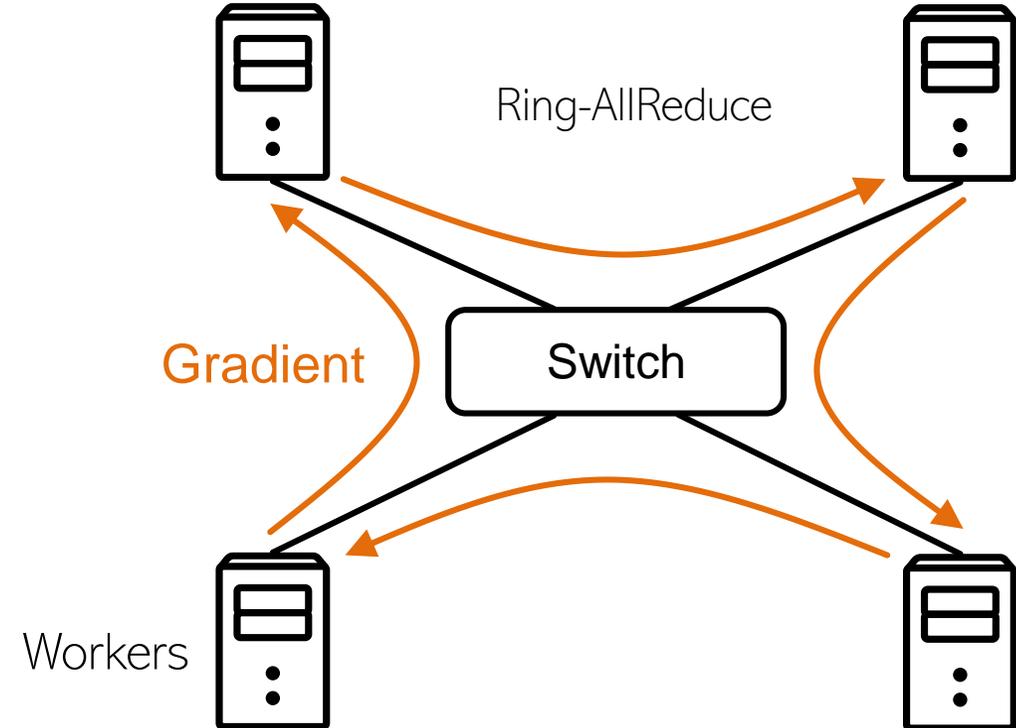


Network Communication is the Bottleneck in Distributed RL Training

Centralized Design

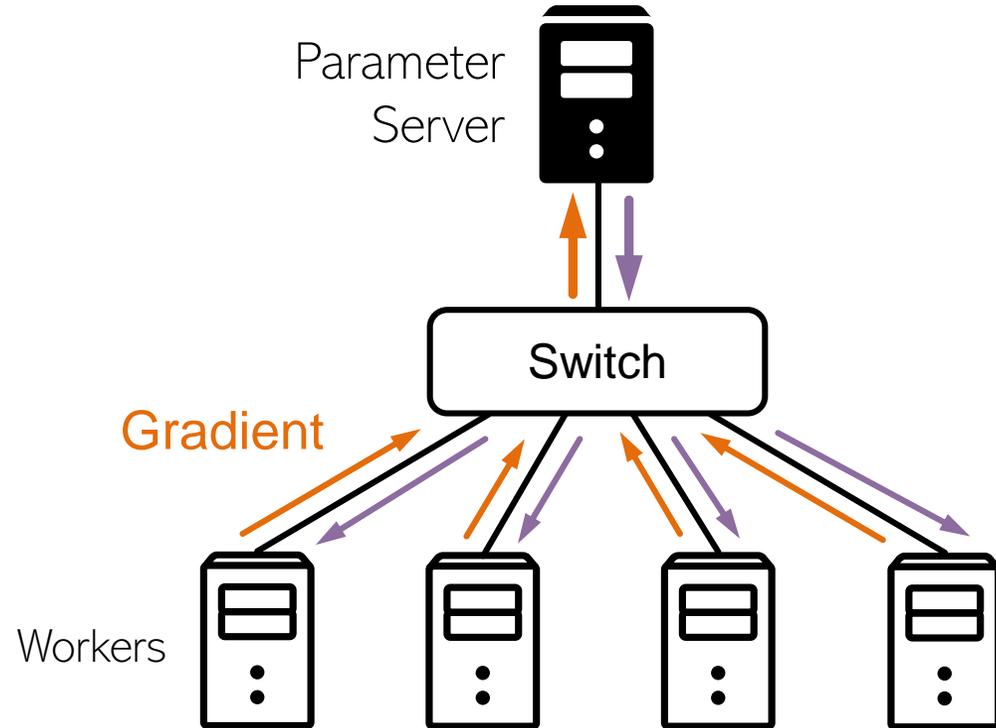


Decentralized Design



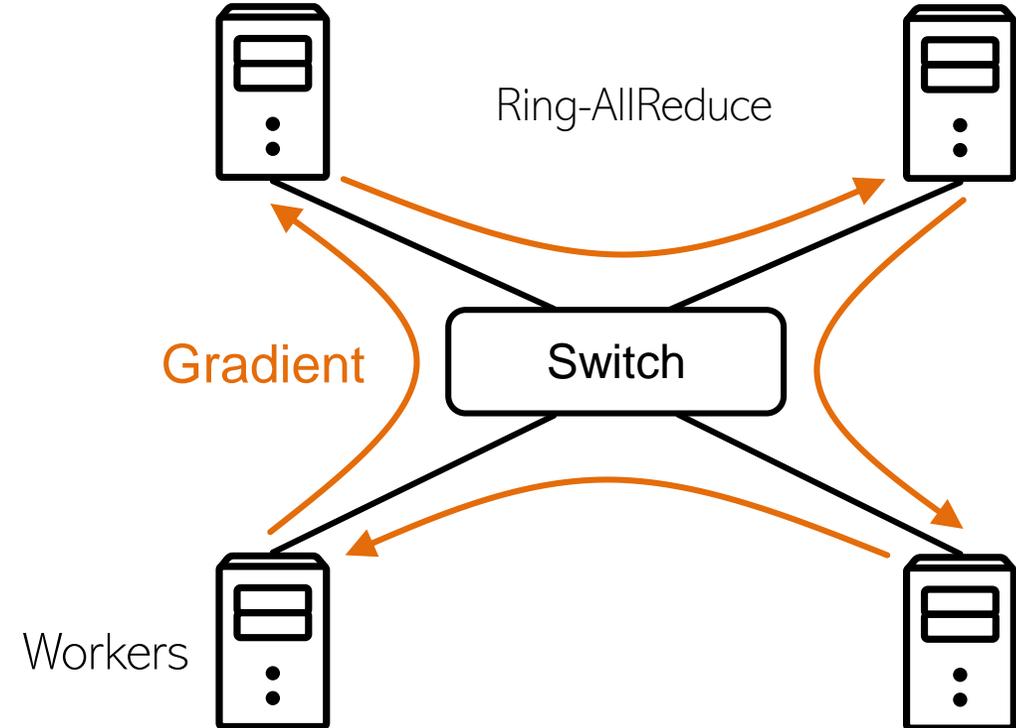
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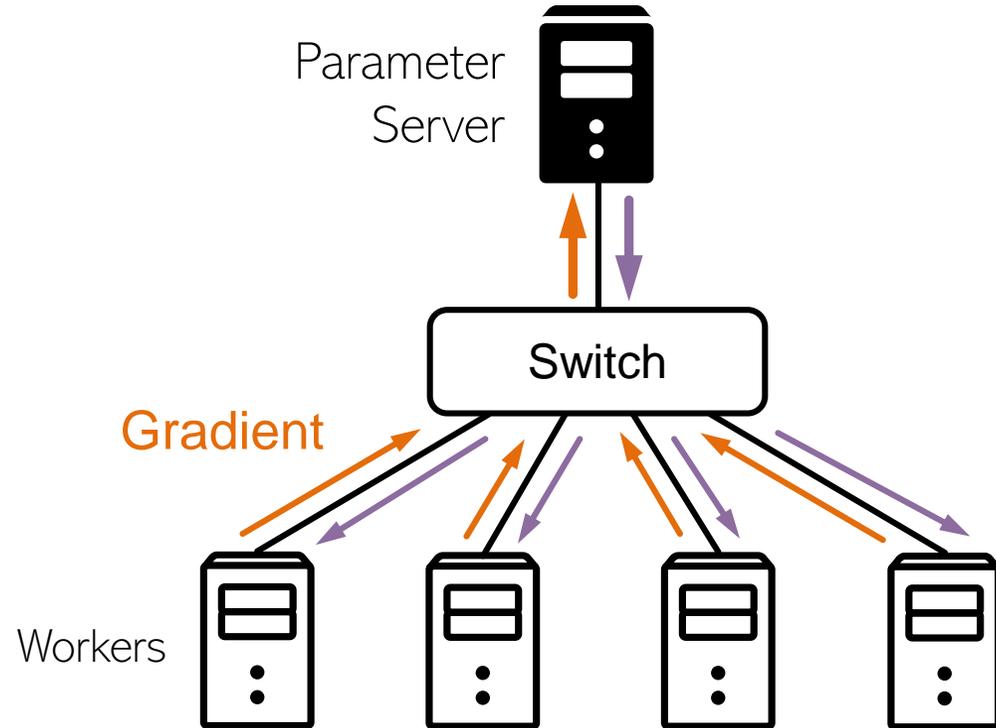
Network Hops = 4

Decentralized Design



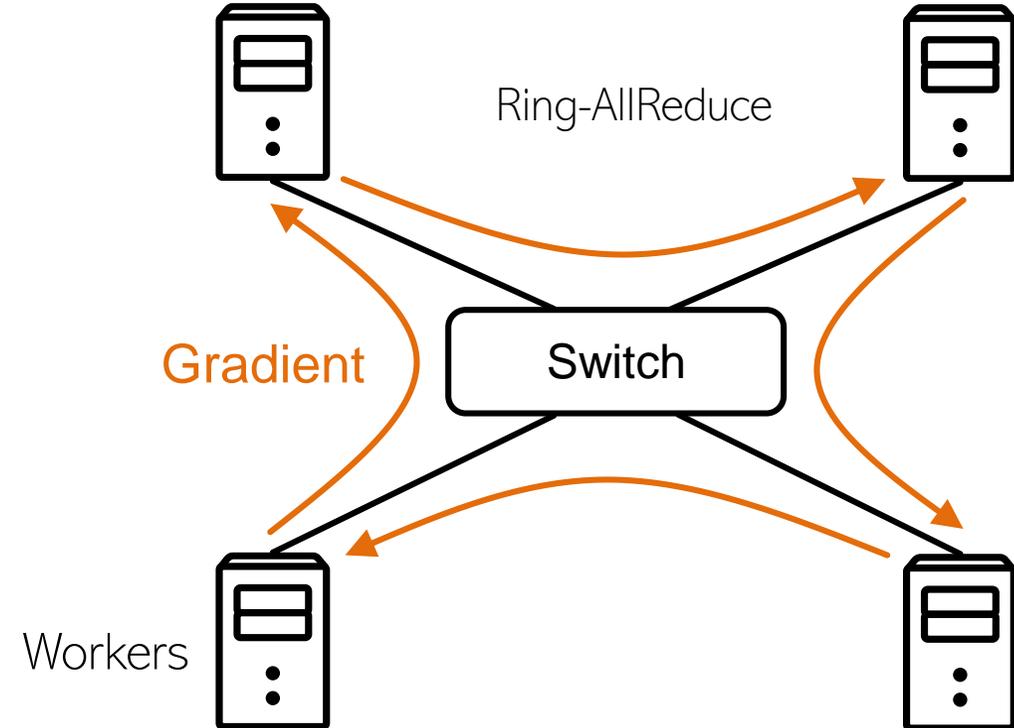
Network Communication is the Bottleneck in Distributed RL Training

Centralized Design



Network Hops = 4

Decentralized Design



Network Hops = $4N - 4$

The Unique Characteristic of Distributed RL Training: Latency Critical

RL Benchmark	DQN- Atari	A2C- Atari	PPO- MuJoCo	DDPG- MuJoCo
Gradient Size	6 MB	3 MB	40 KB	158 KB
Training Iterations	200 M	2 M	0.2 M	3 M

The Unique Characteristic of Distributed RL Training: Latency Critical

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88x Smaller
Gradient Size

158x More
Iterations

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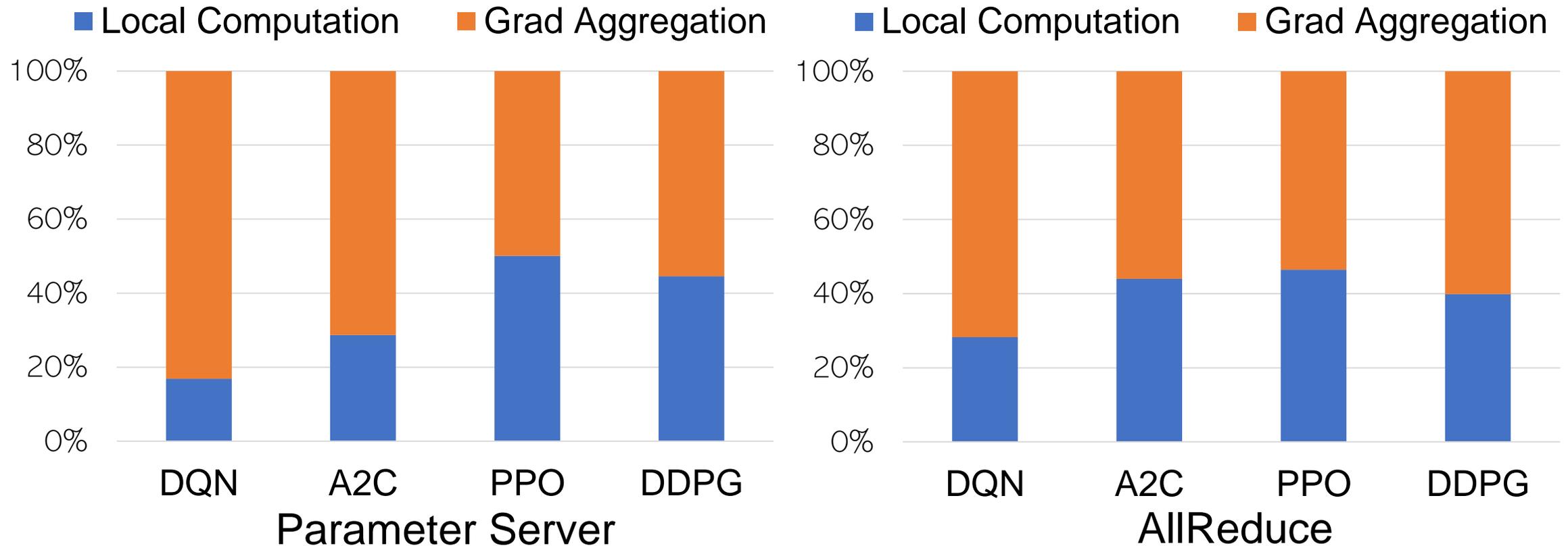
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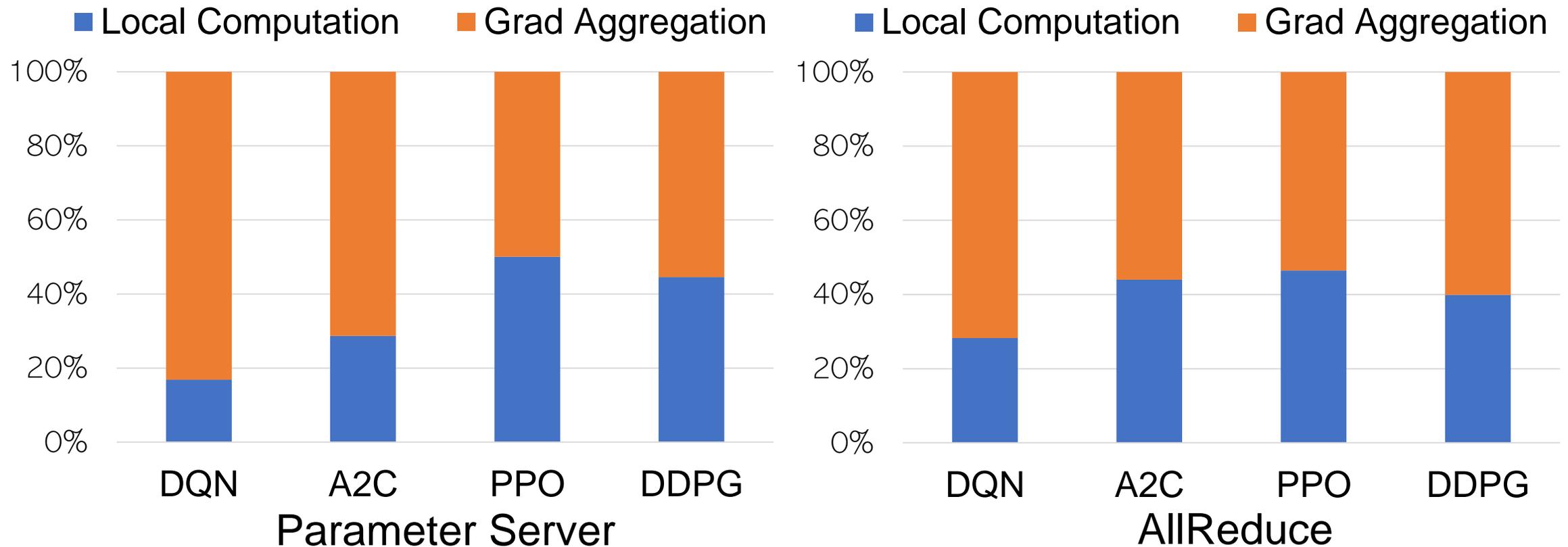
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Iterations

Distributed RL Training is Latency Critical

Quantifying the Network Overhead in Distributed RL Training

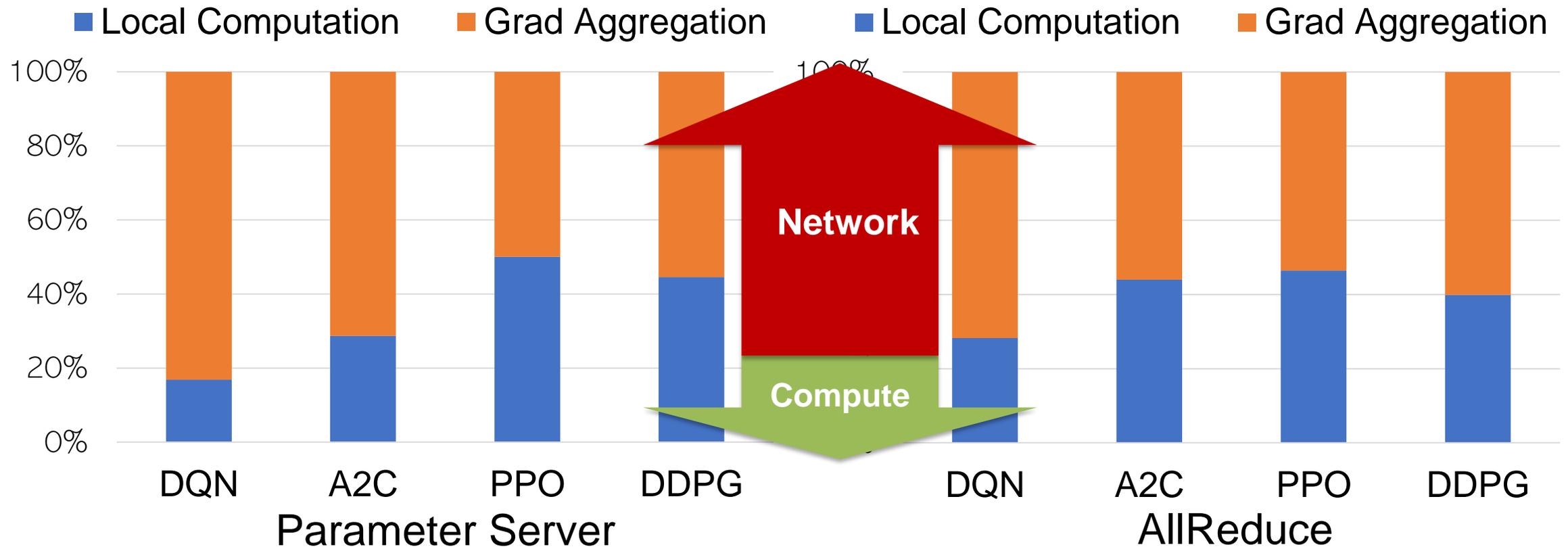


Quantifying the Network Overhead in Distributed RL Training



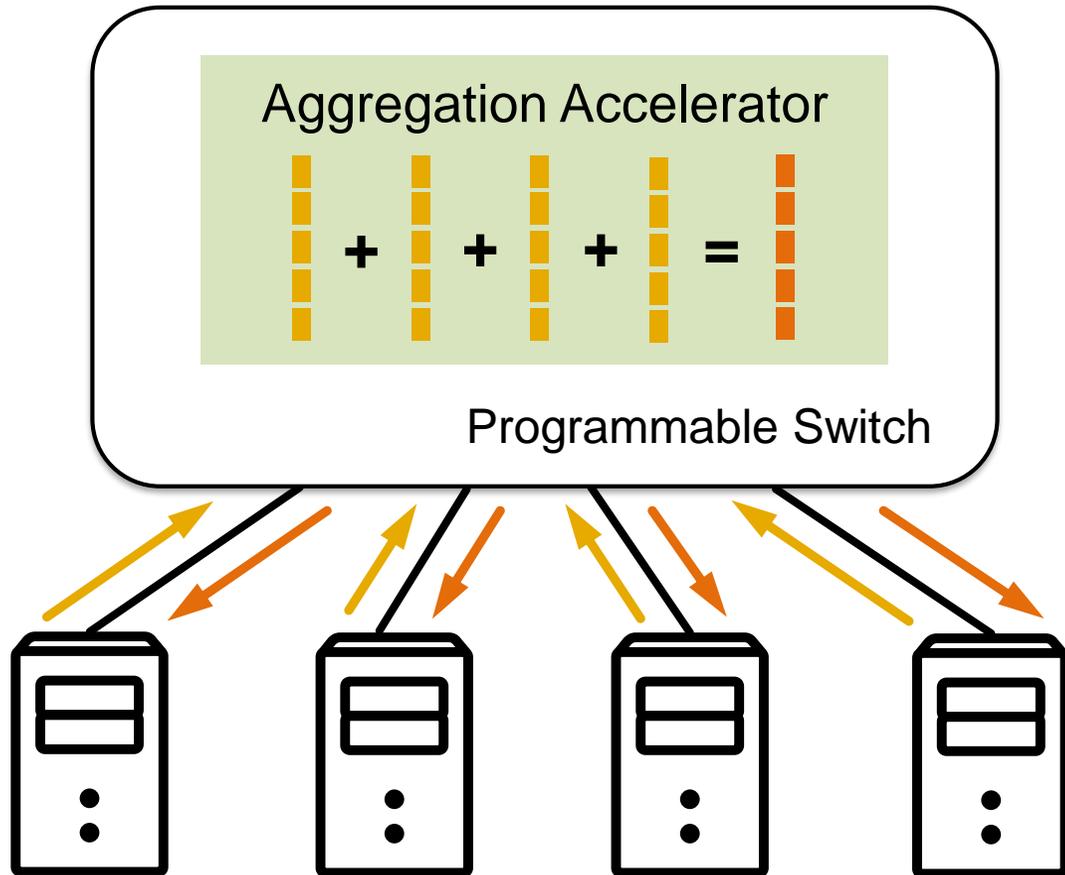
Gradient Aggregation over the Network Dominates the Training Time (50~83%)

Quantifying the Network Overhead in Distributed RL Training

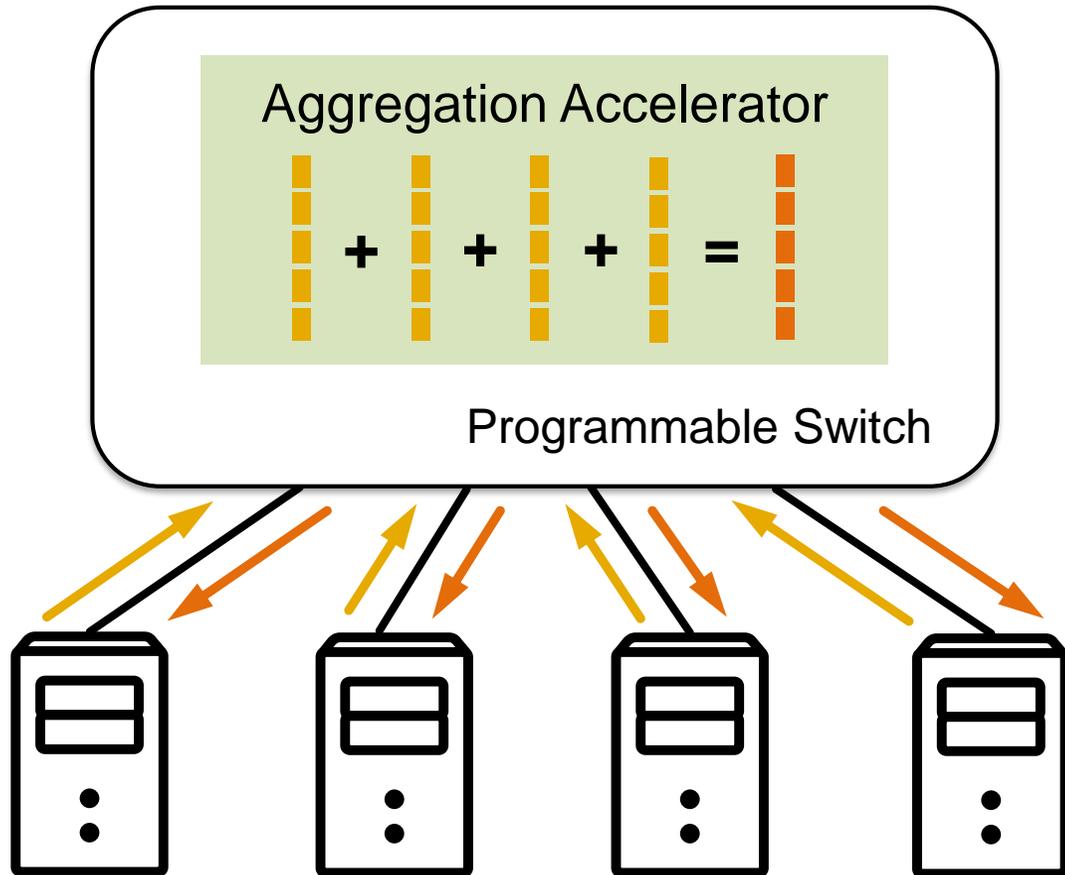


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In-Switch Acceleration: A New Distributed Computing Paradigm



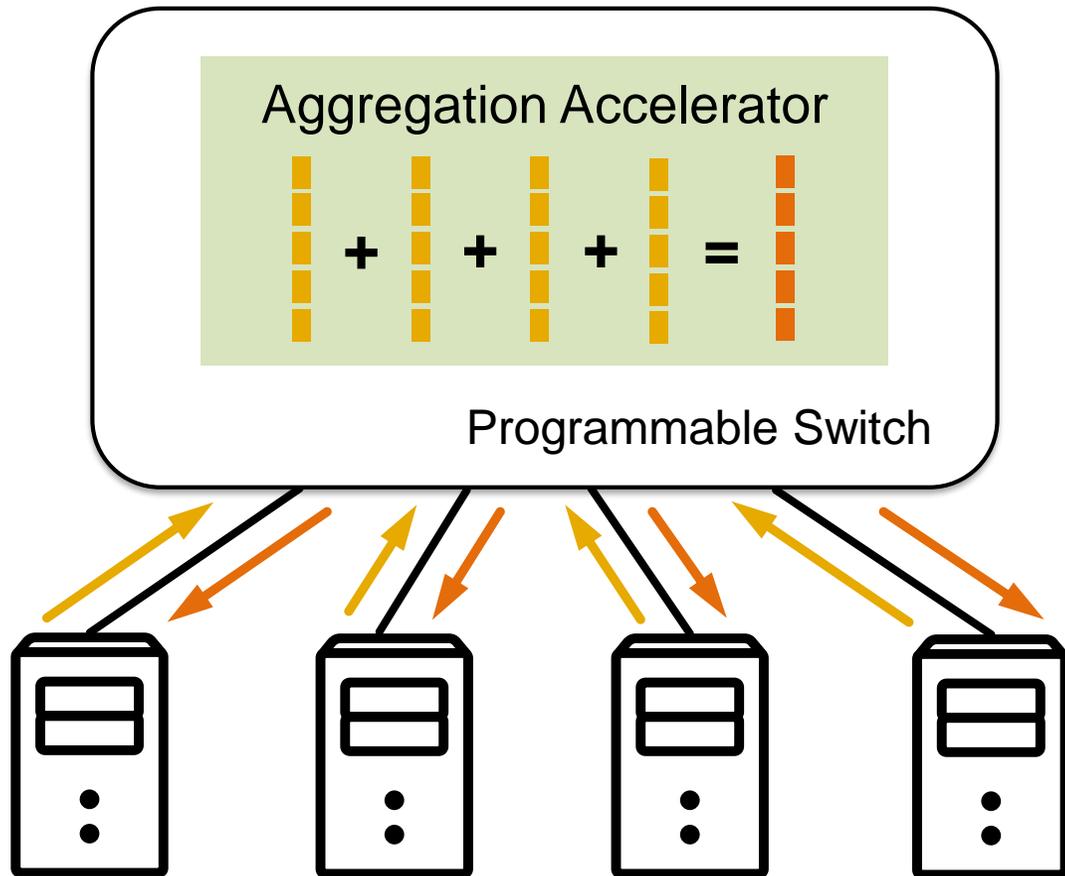
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Performance

Reduce End-to-End Network Latency

In-Switch Acceleration: A New Distributed Computing Paradigm



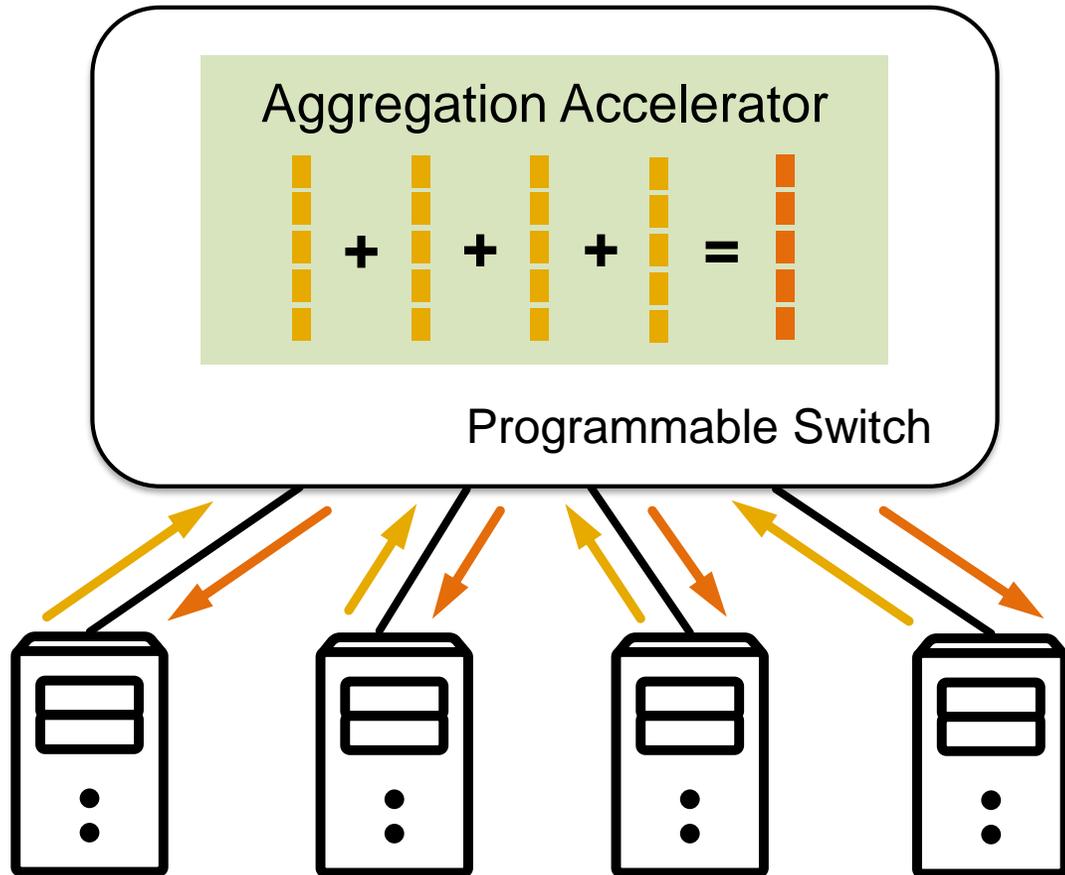
Performance

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Programmability

Hardware-Algorithm Co-Design

In-Switch Acceleration: A New Distributed Computing Paradigm



Performance

Reduce End-to-End Network Latency

Programmability

Hardware-Algorithm Co-Design

Scalability

Scale Training at Rack Scale

Challenges of In-Switch Acceleration

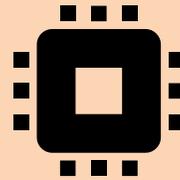


No Impact on
Regular Switch
Functions

Challenges of In-Switch Acceleration



No Impact on
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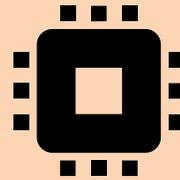


Limited
On-Chip
Resources

Challenges of In-Switch Acceleration



No Impact on
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Functions



Limited
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Resources



Scale with
More Switches
and Nodes

Basics of Programmable Switch

Control Plane



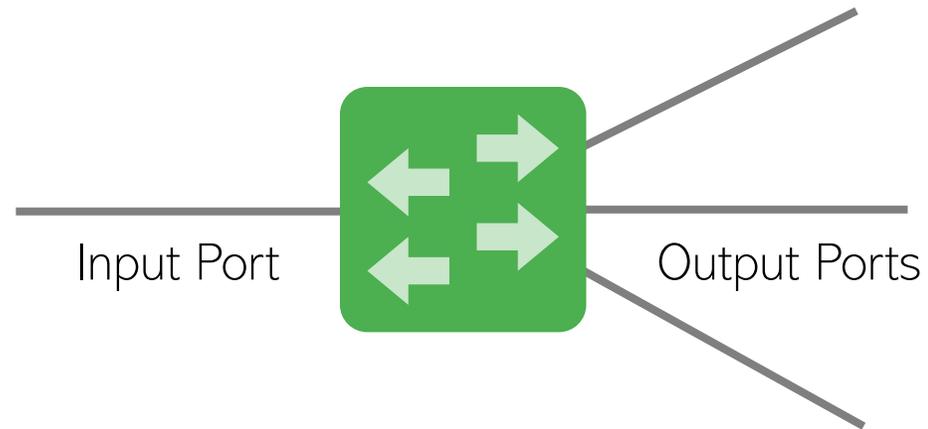
Data Plane

Basics of Programmable Switch

Control Plane



Data Plane

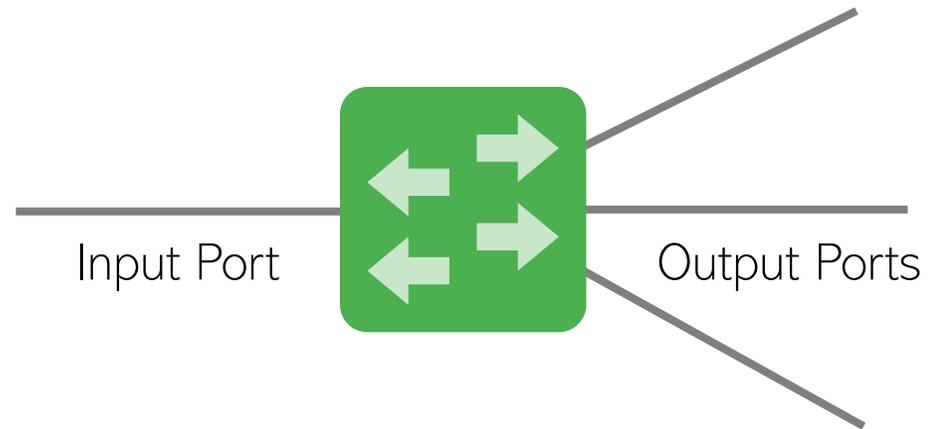


Basics of Programmable Switch

Control Plane



Data Plane

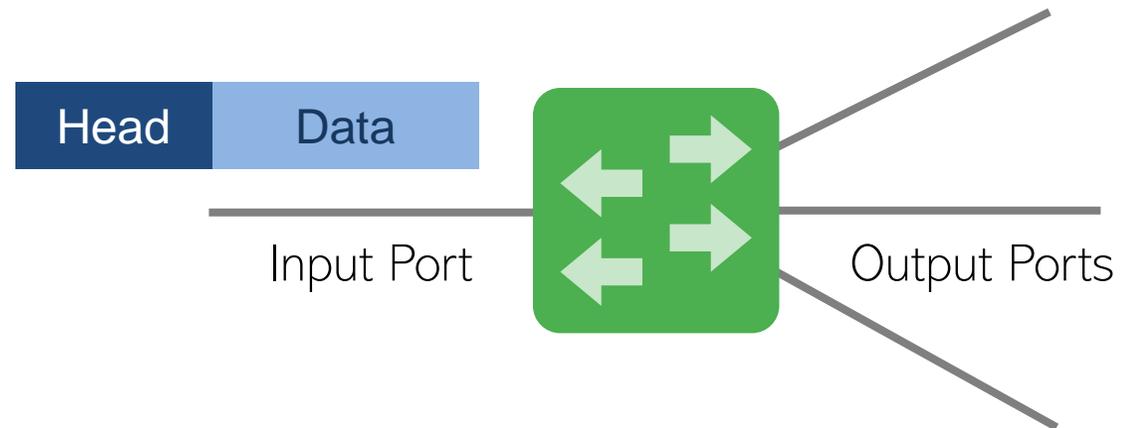


Basics of Programmable Switch

Control Plane



Data Plane

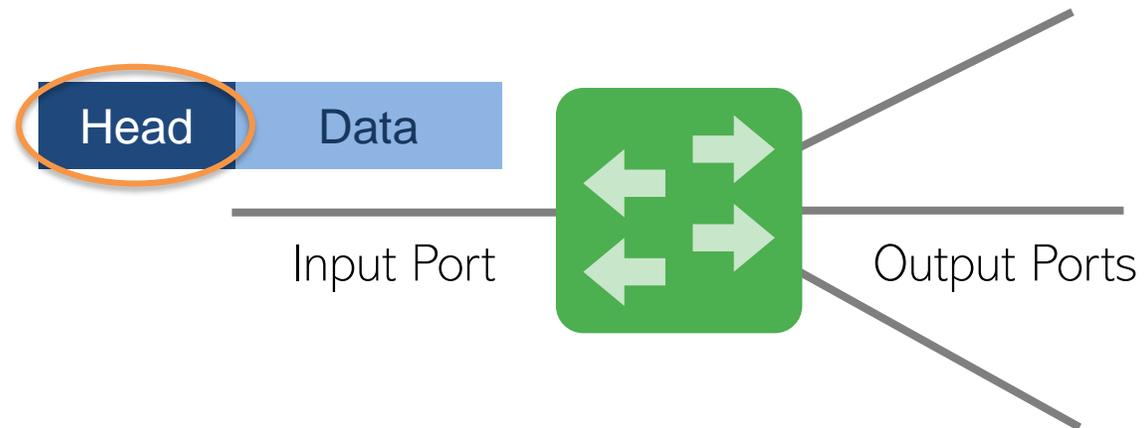


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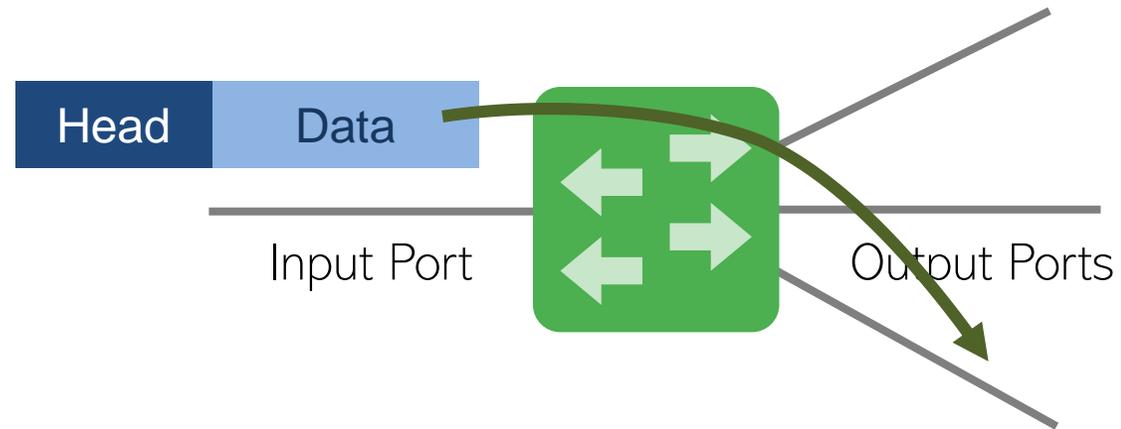


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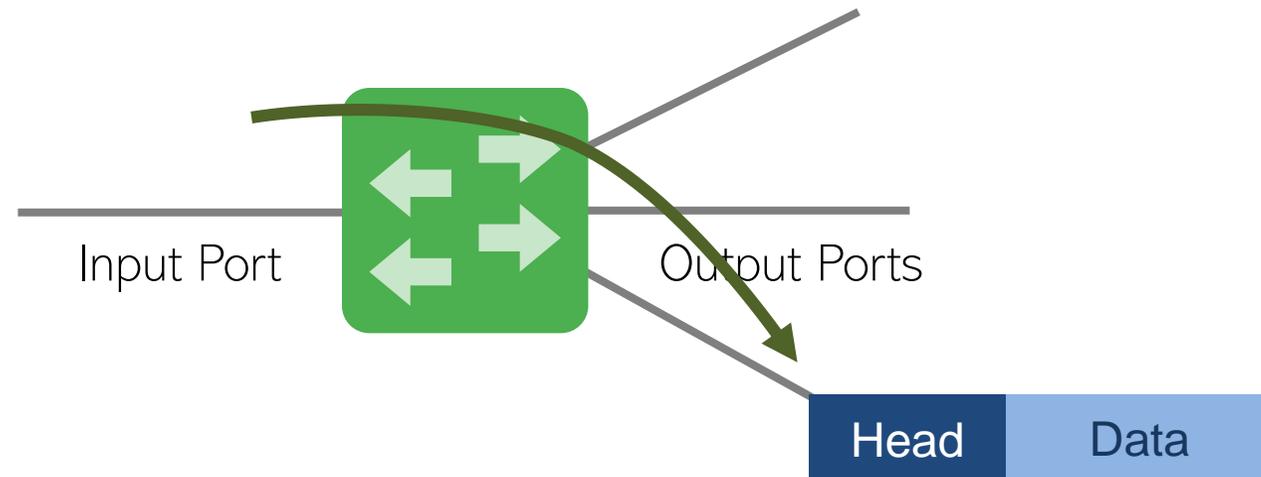


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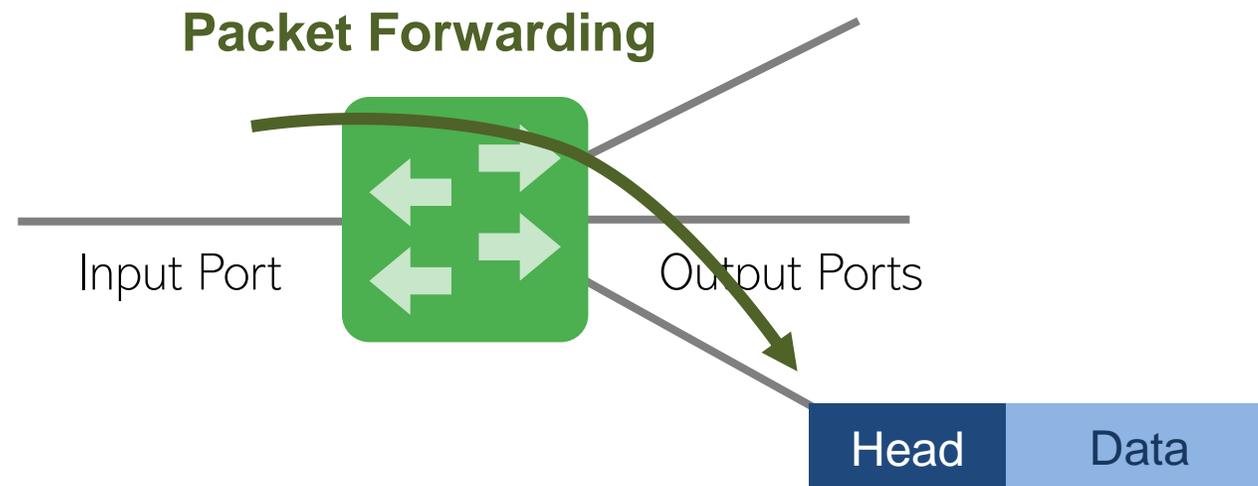


Basics of Programmable Switch

Control Plane



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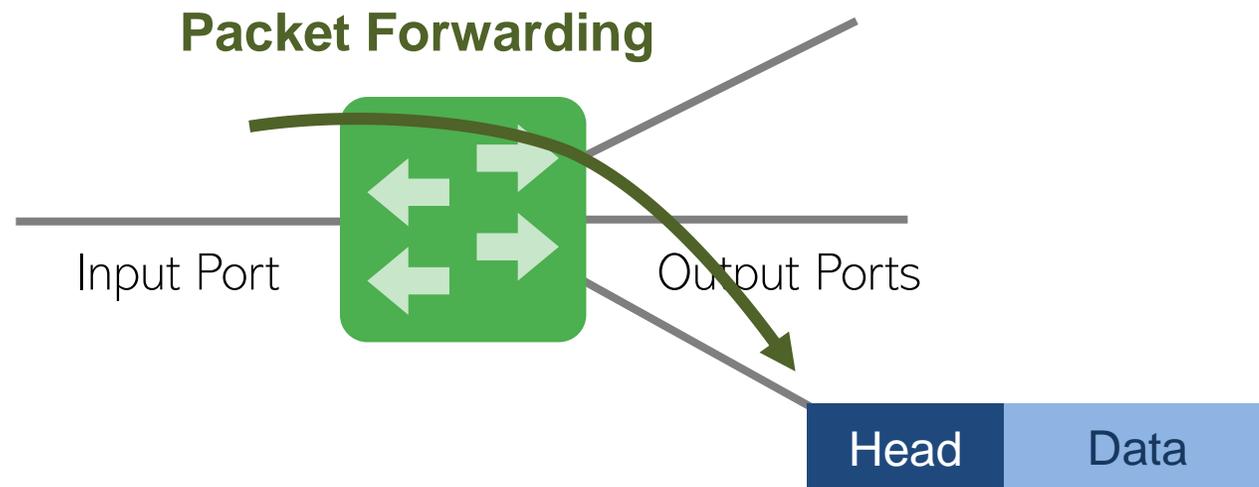


Basics of Programmable Switch

Control Plane

Forwarding Control

Data Plane



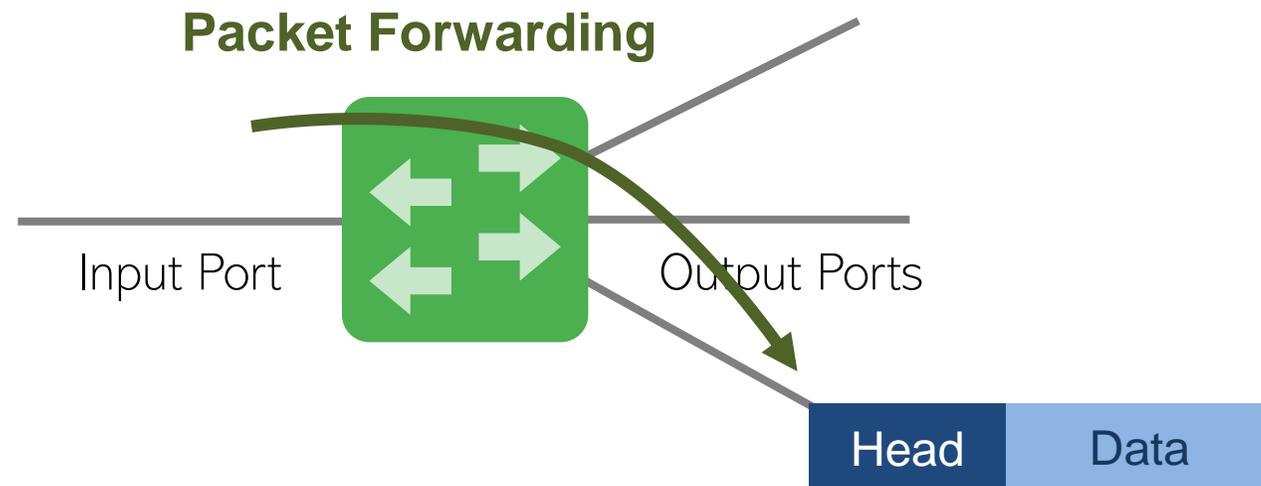
Basics of Programmable Switch

Control Plane

Forwarding Control

System Configuration

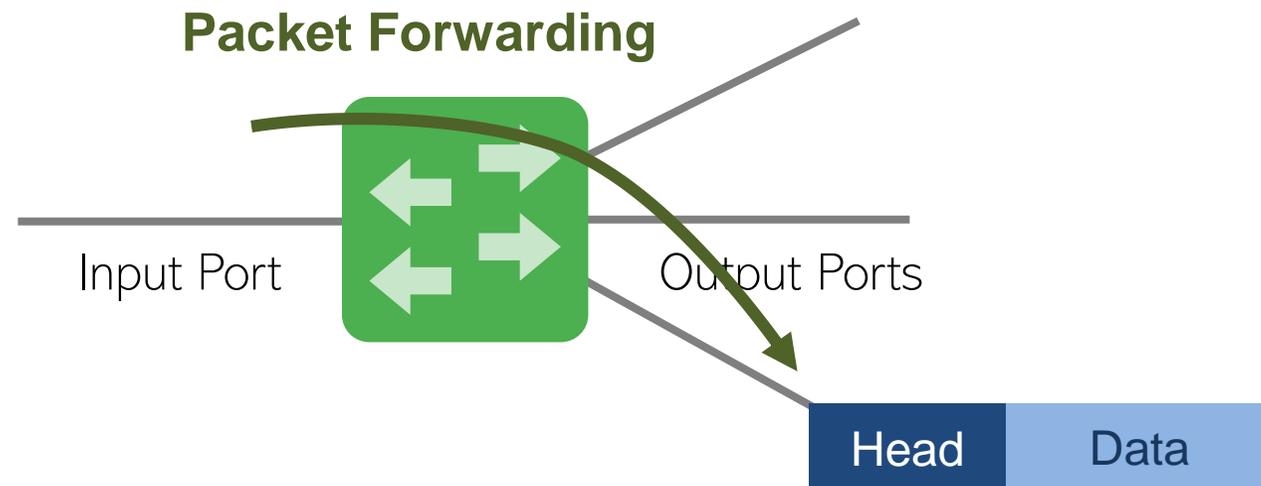
Data Plane



Basics of Programmable Switch



Data Plane



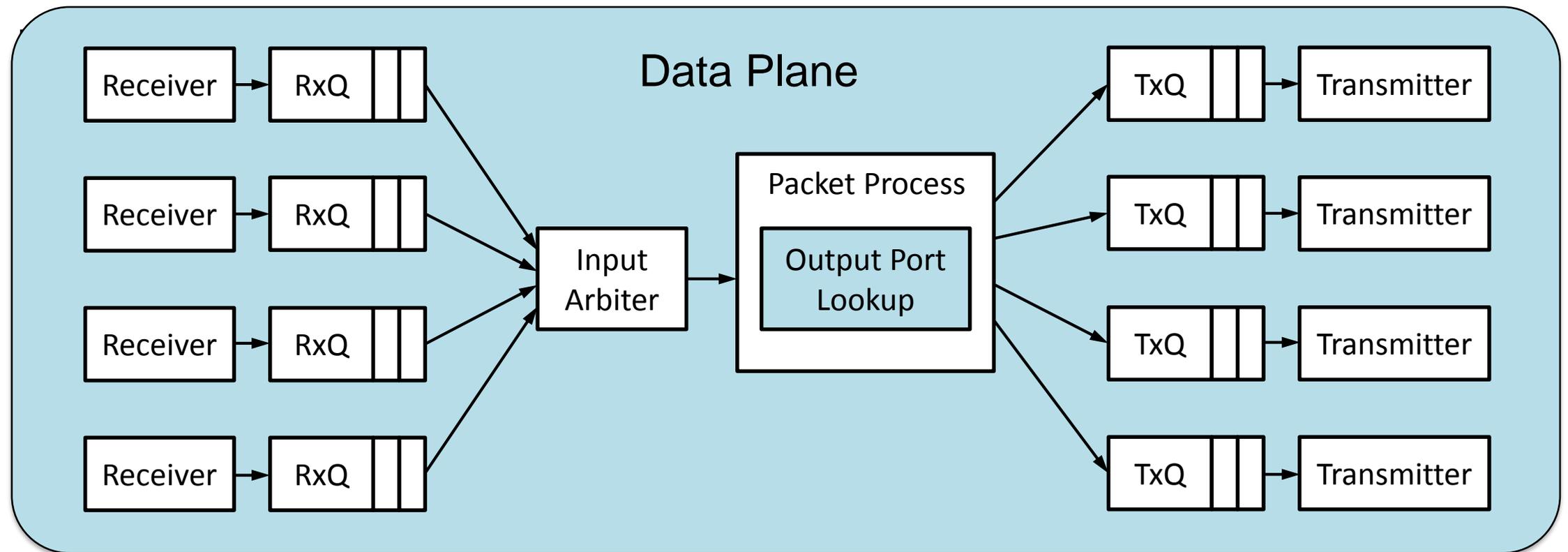
Basics of Programmable Switch

Control Plane

Forwarding Control

System Configuration

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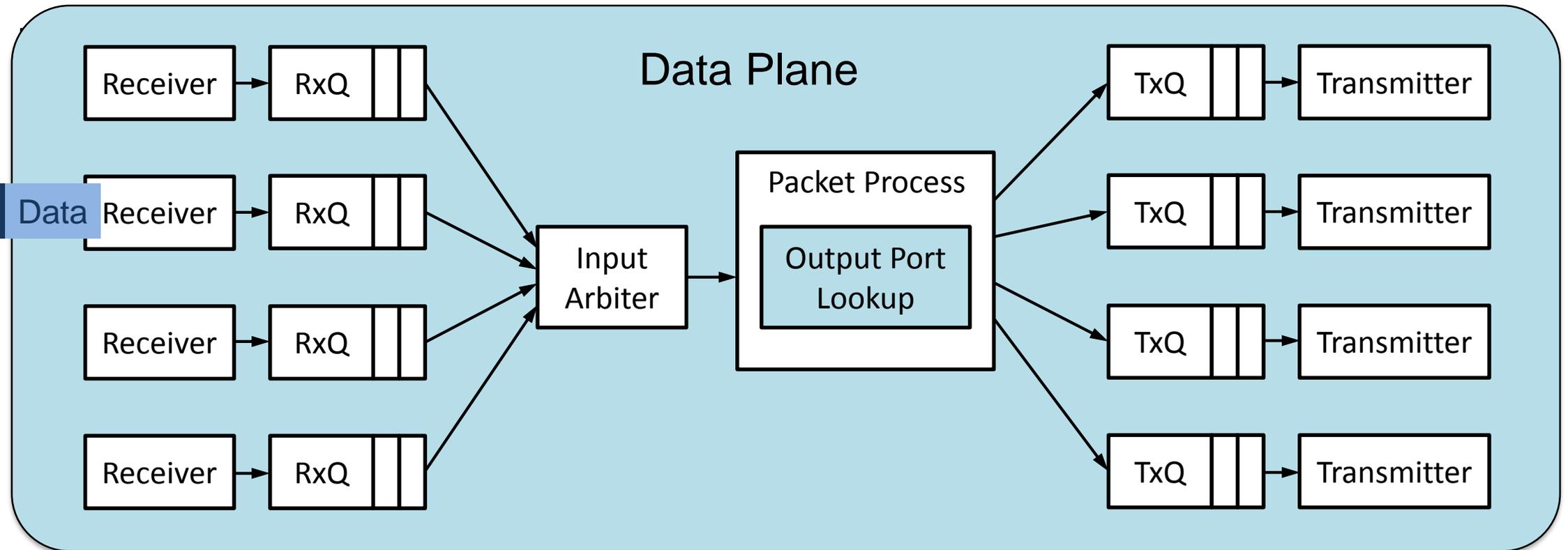
Basics of Programmable Switch

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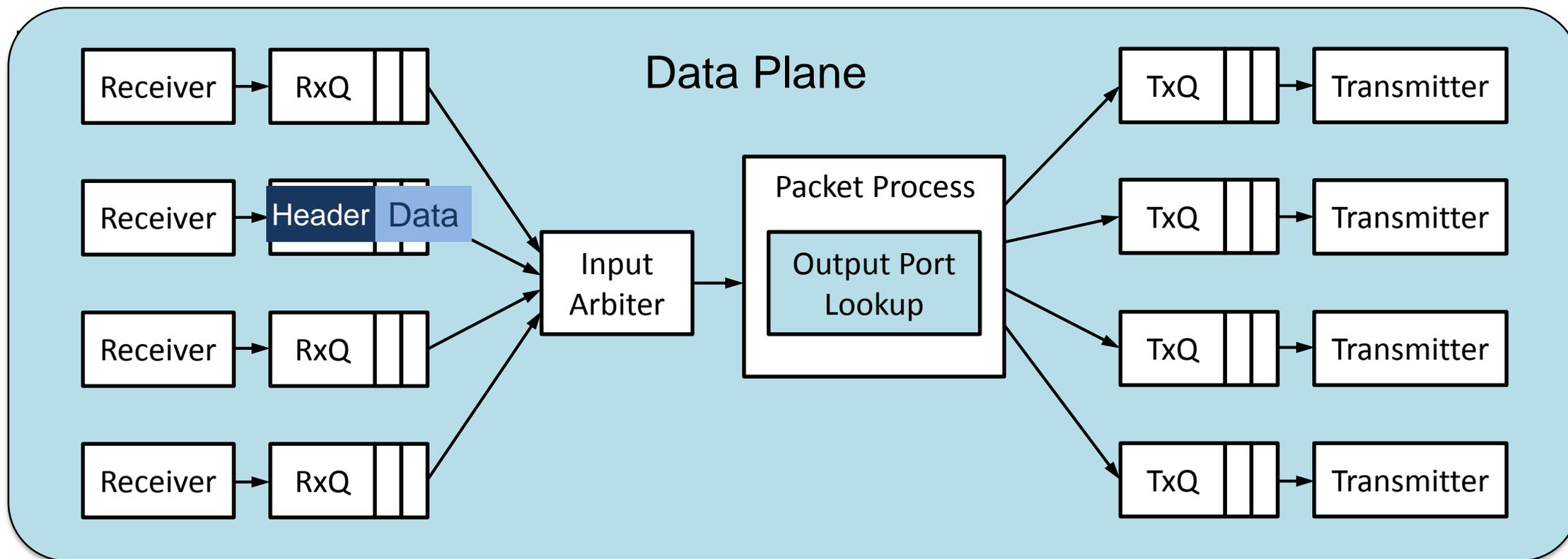
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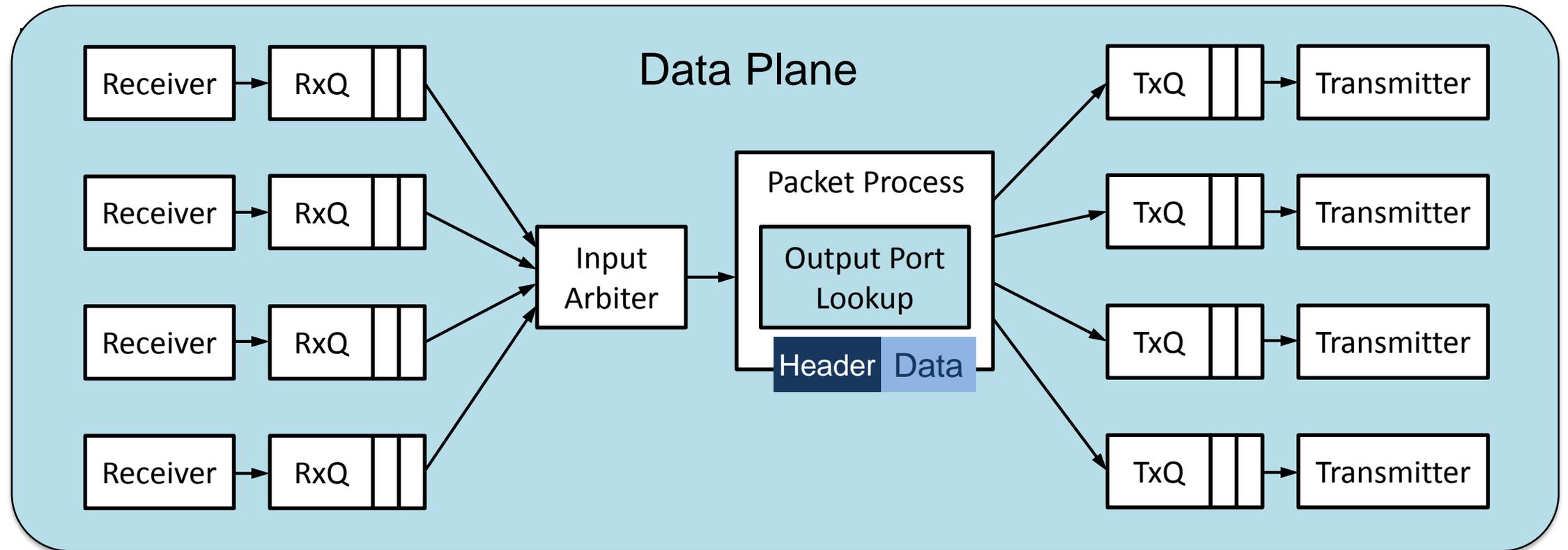
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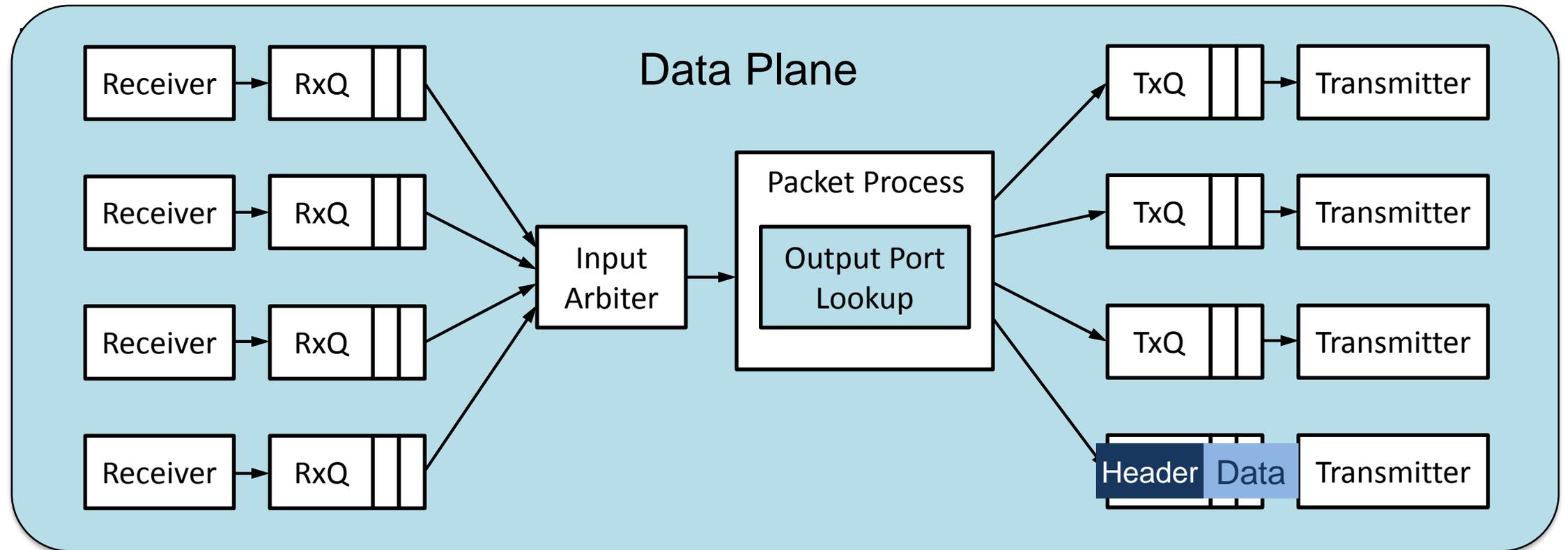
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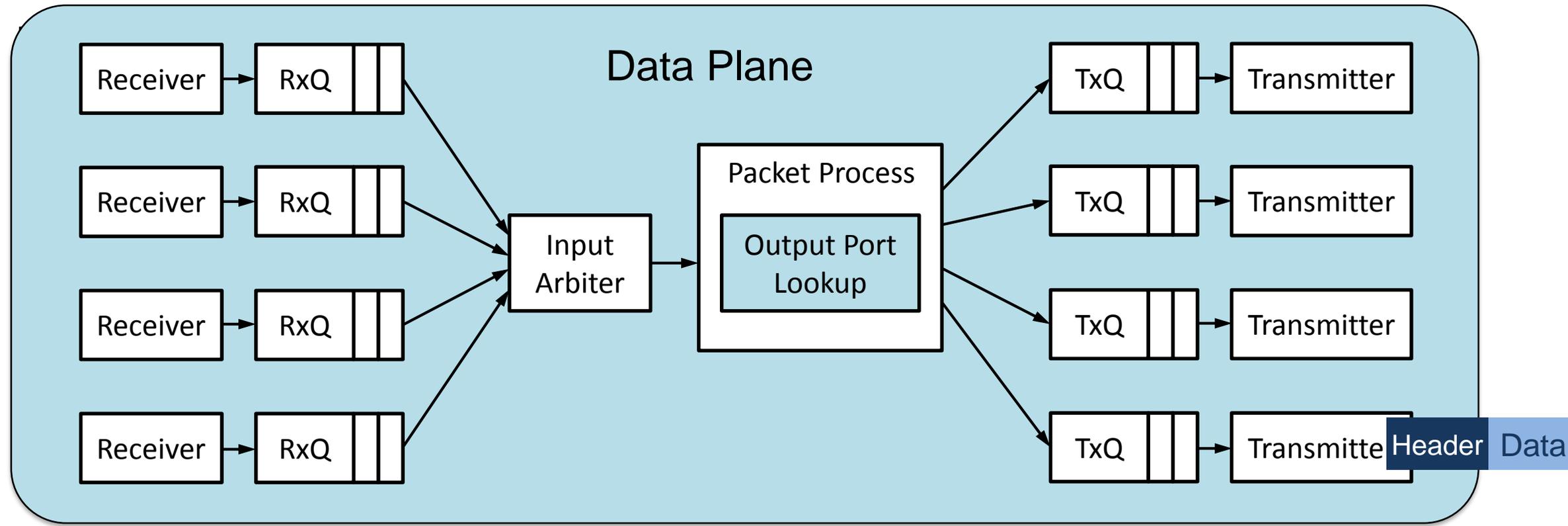
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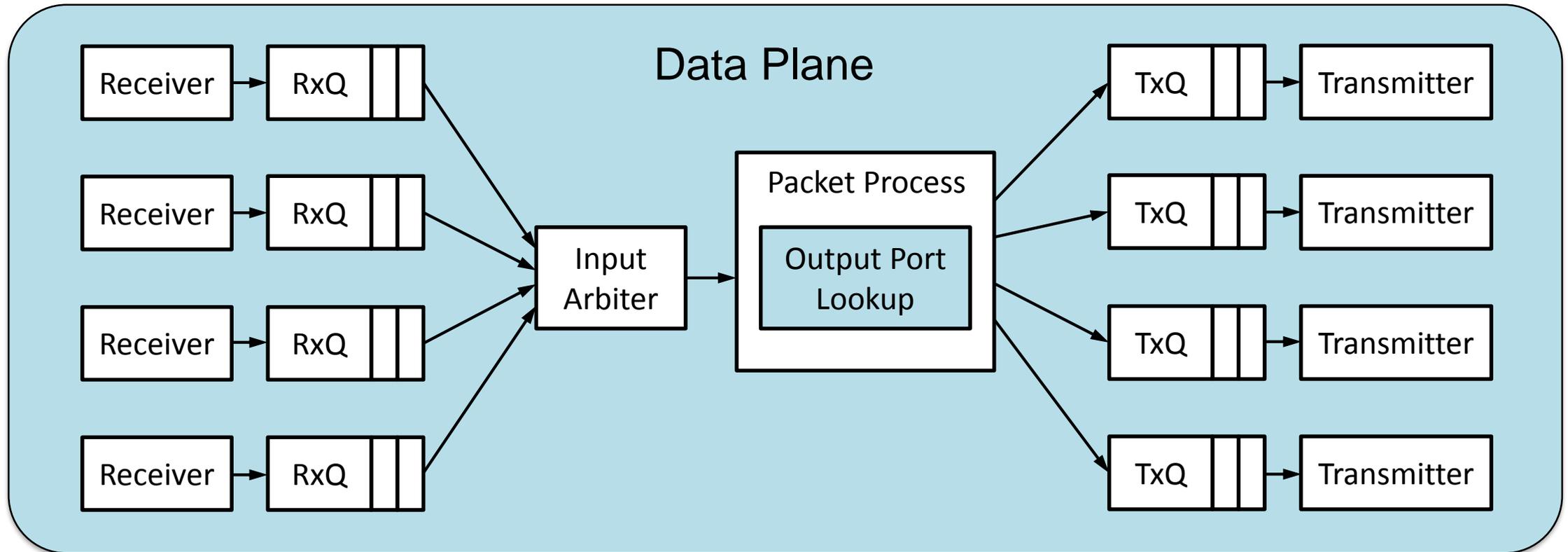
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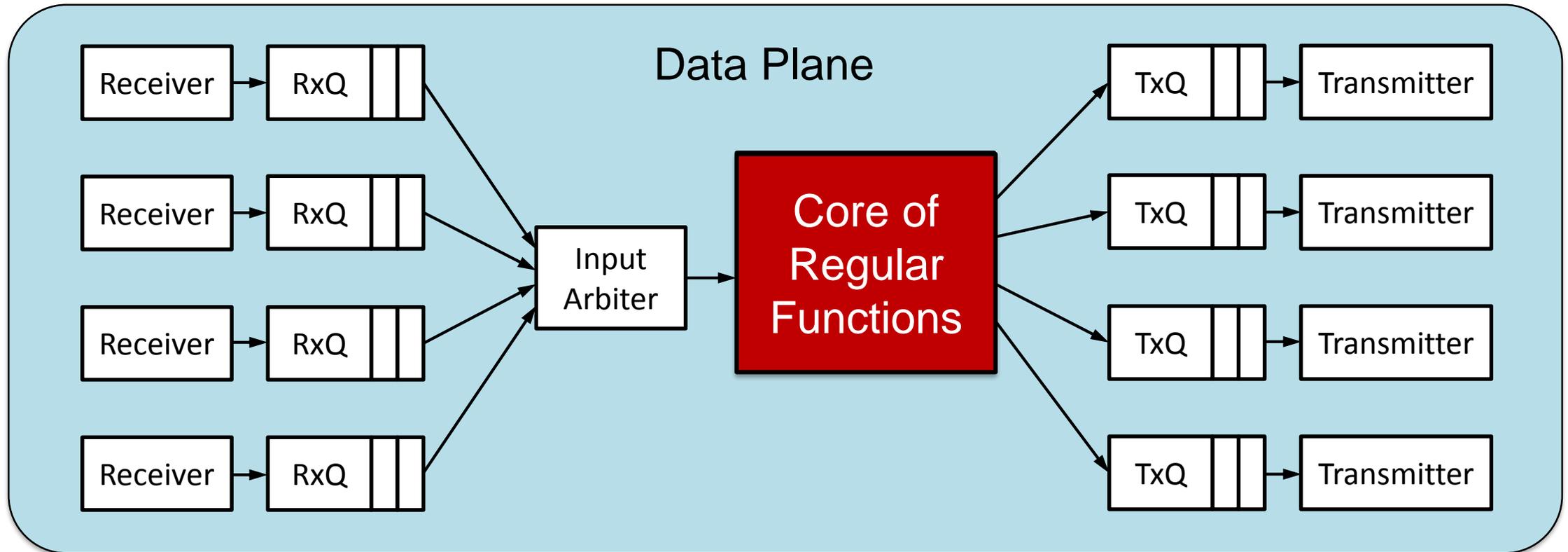
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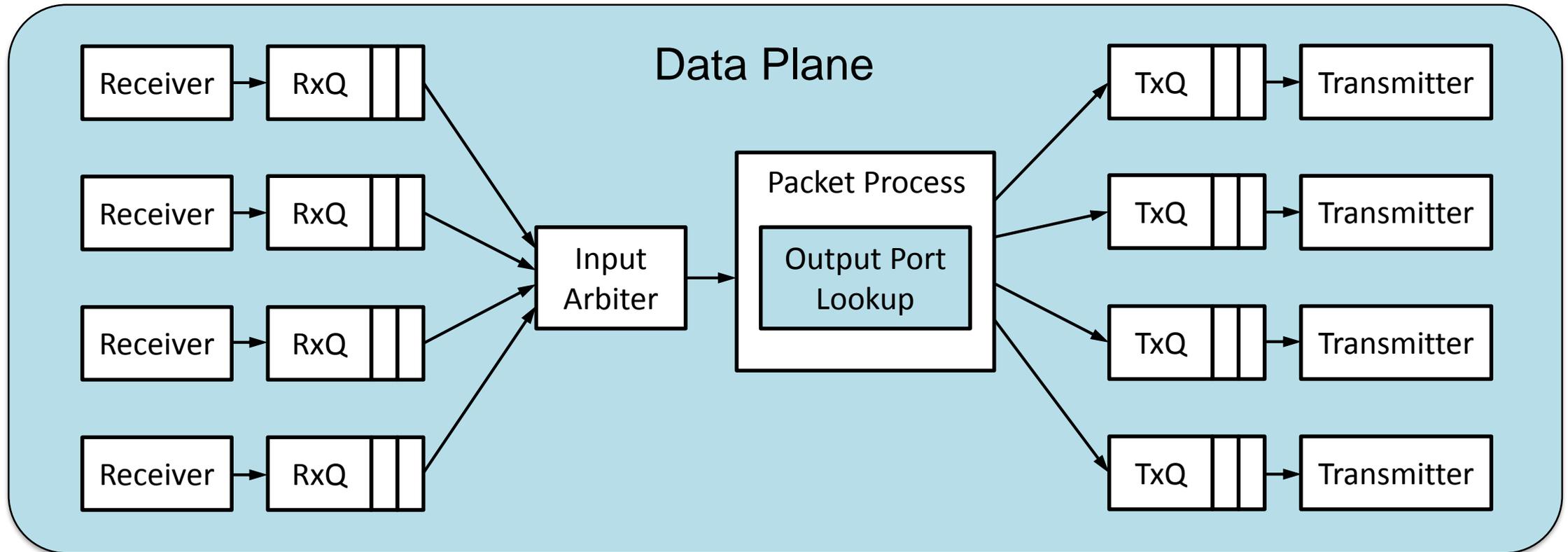
Integrating Aggregation Accelerator into the Programmable Switch



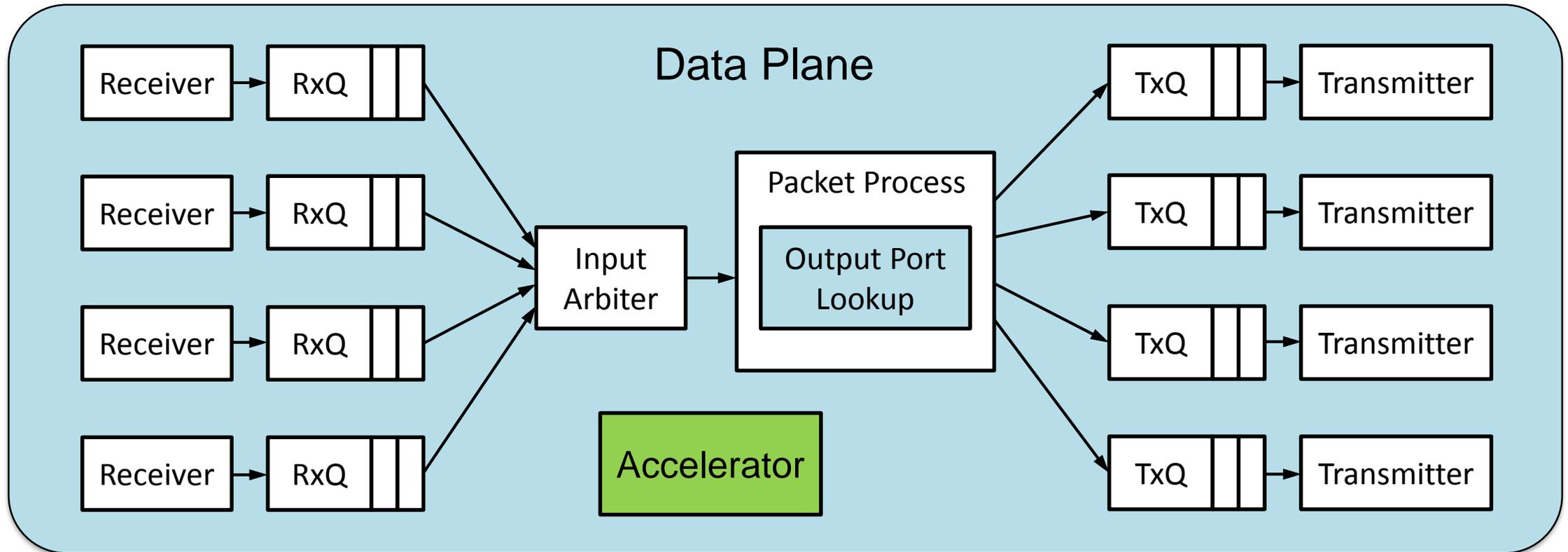
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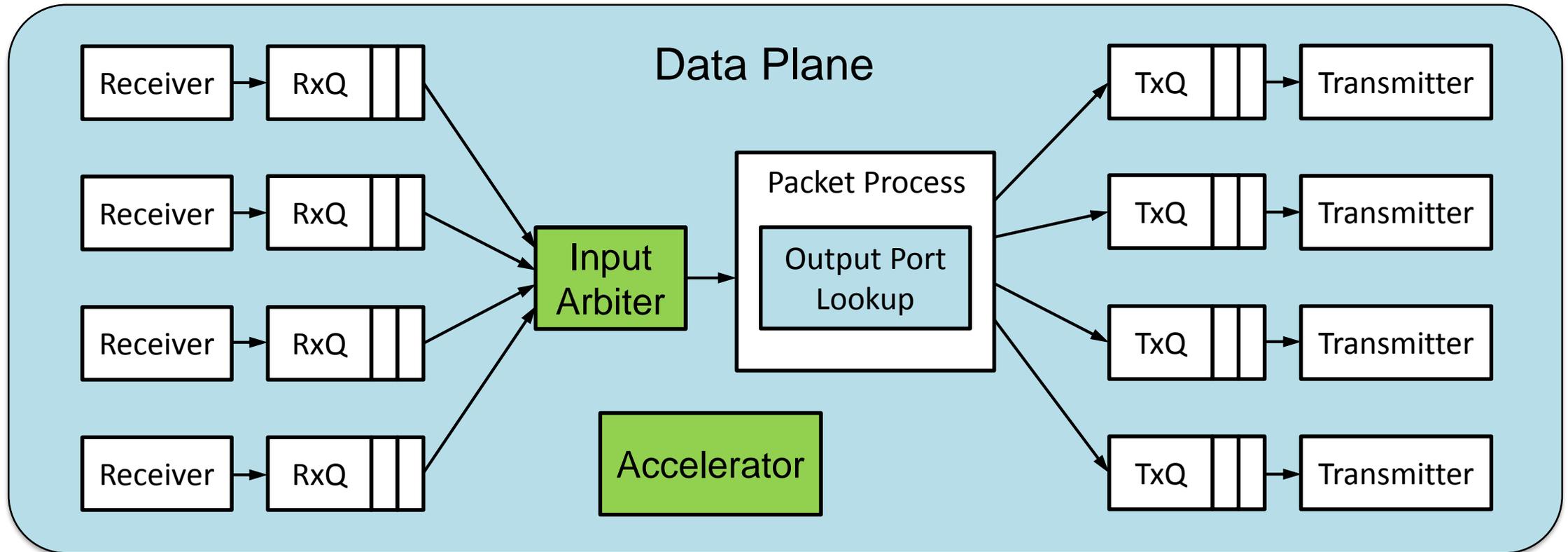
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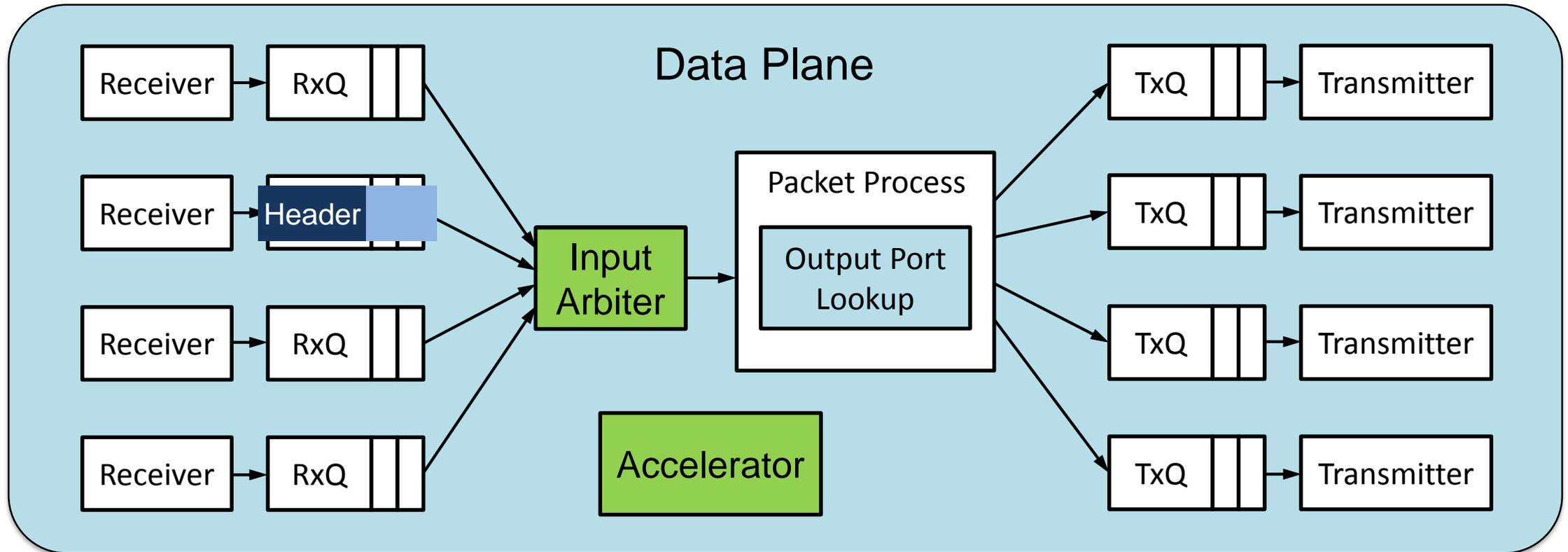
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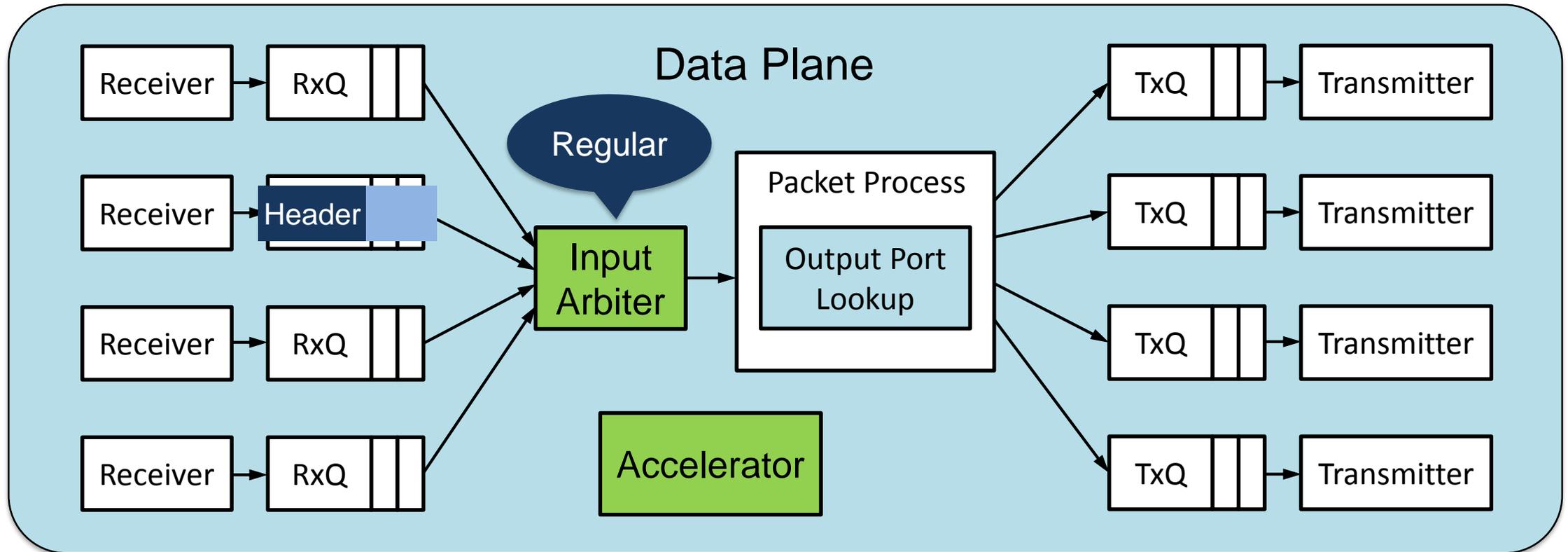
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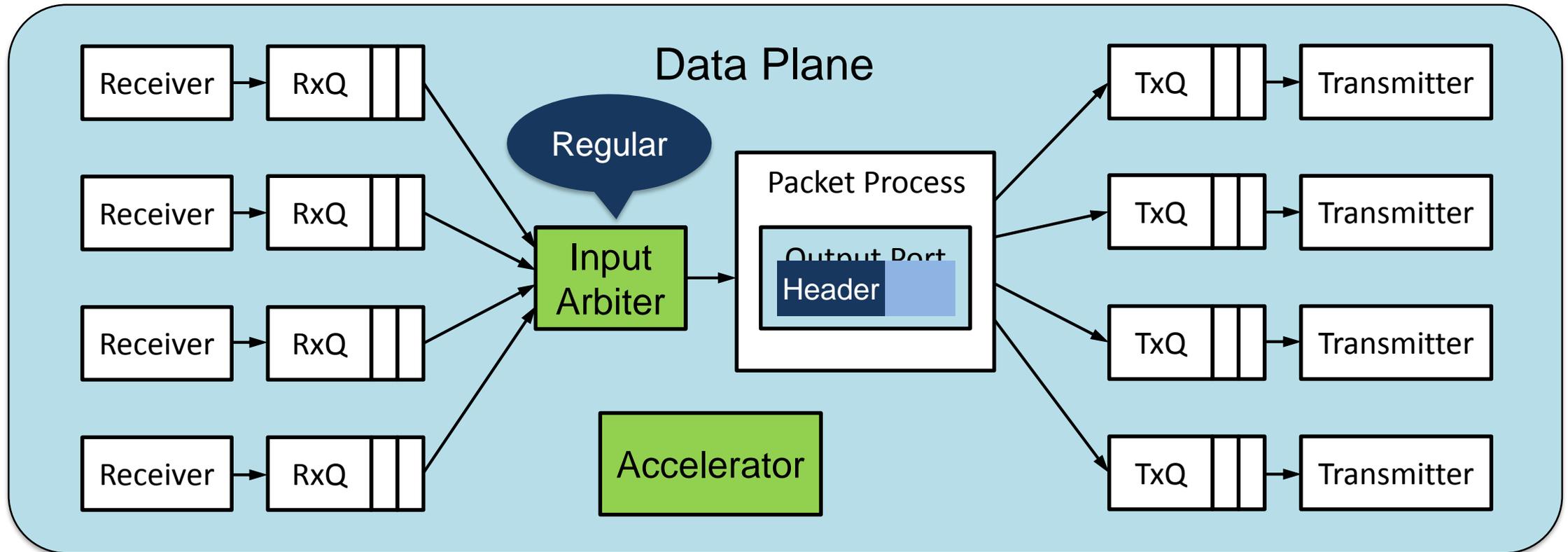
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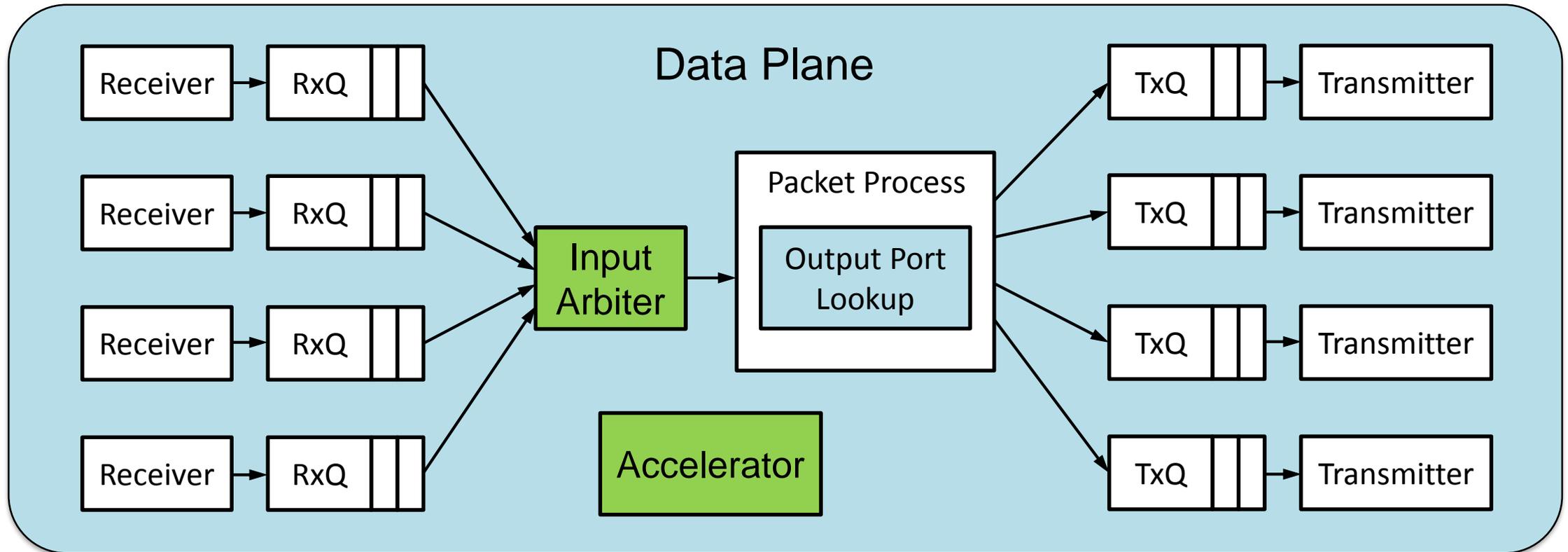
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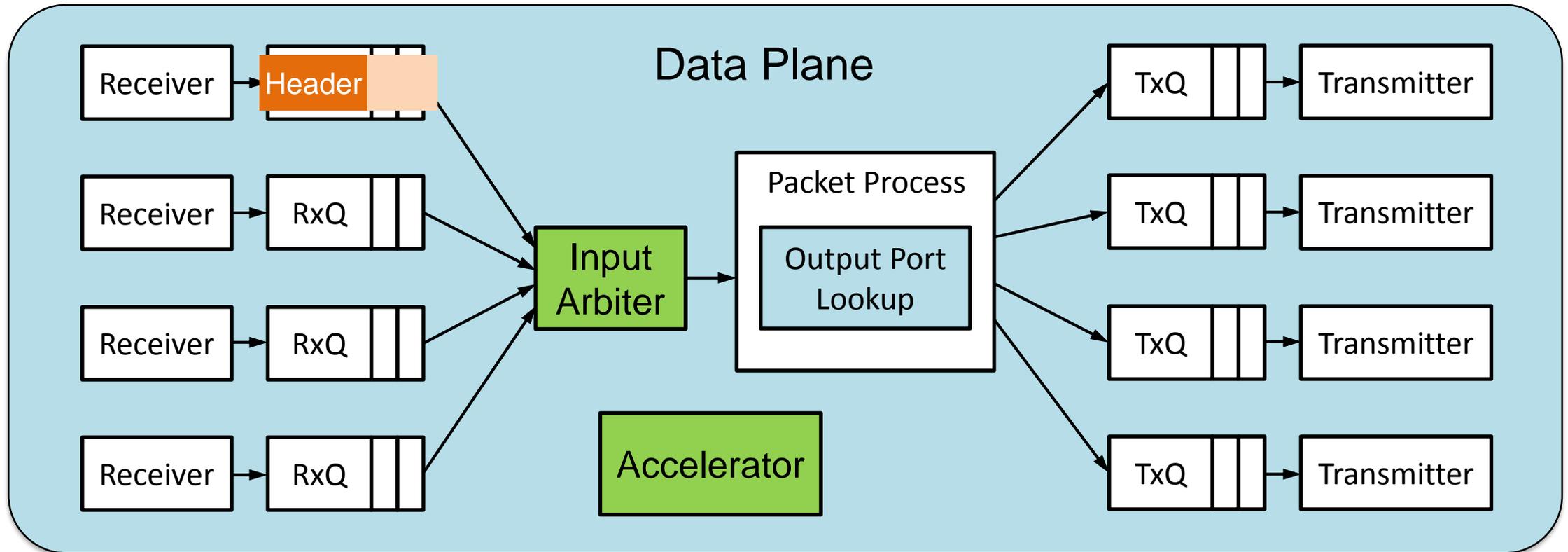
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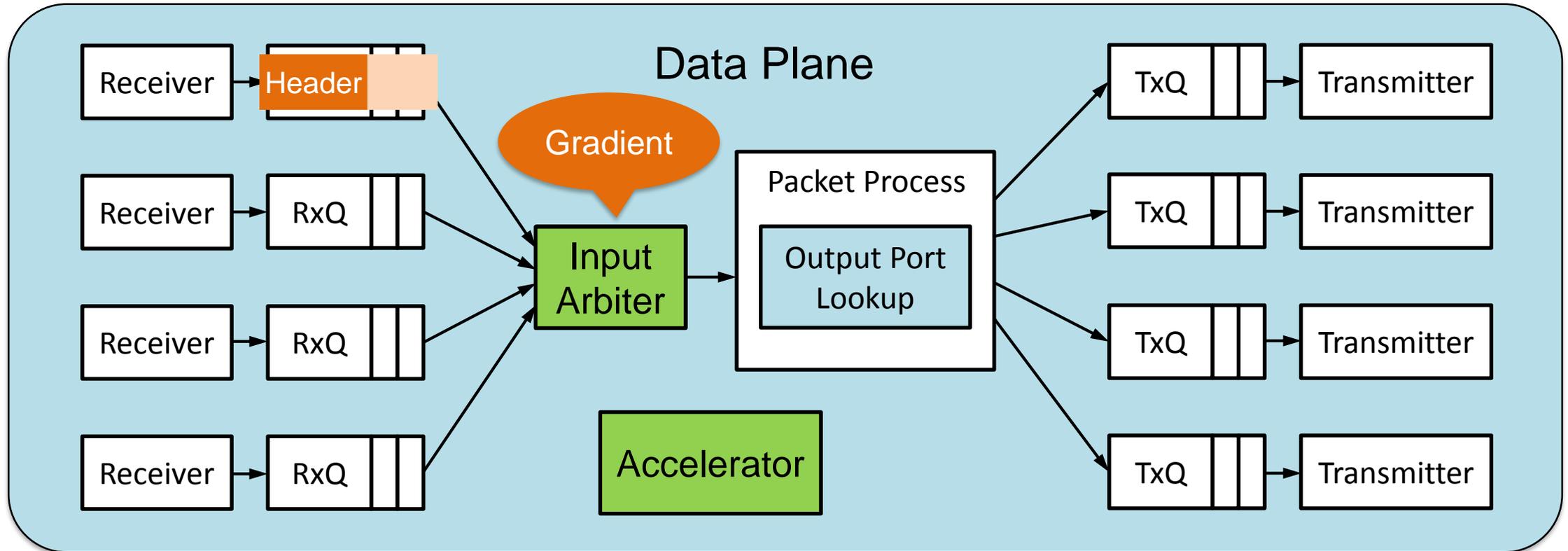
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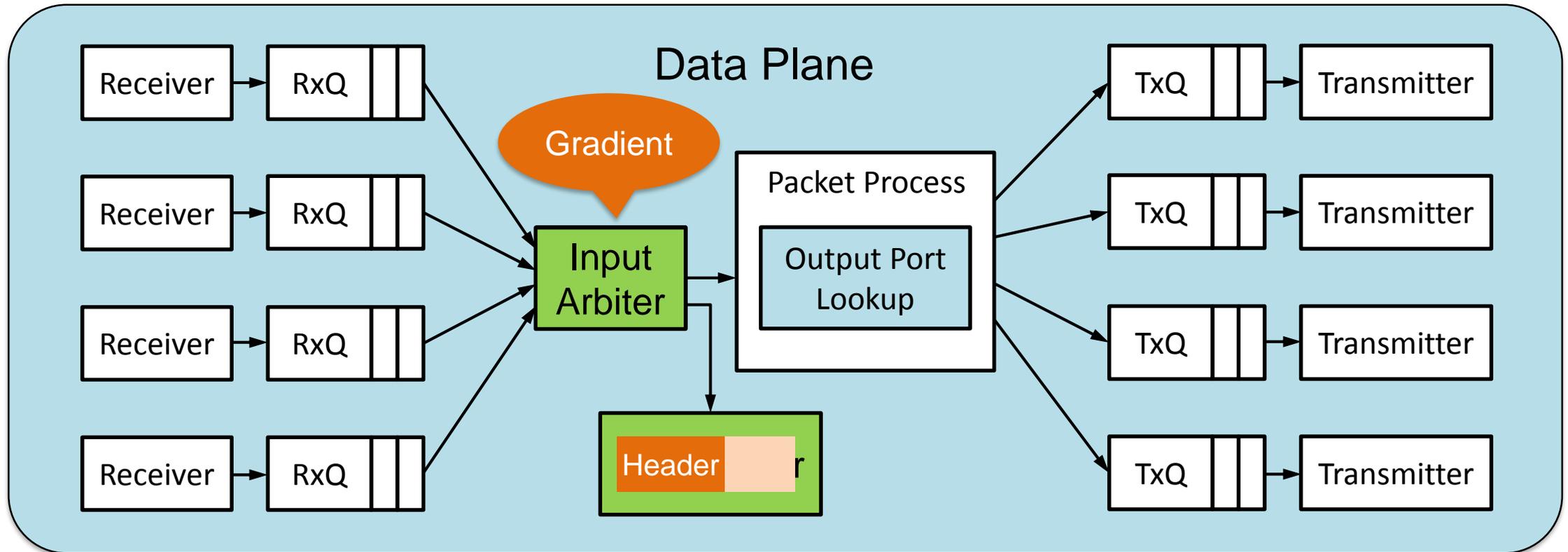
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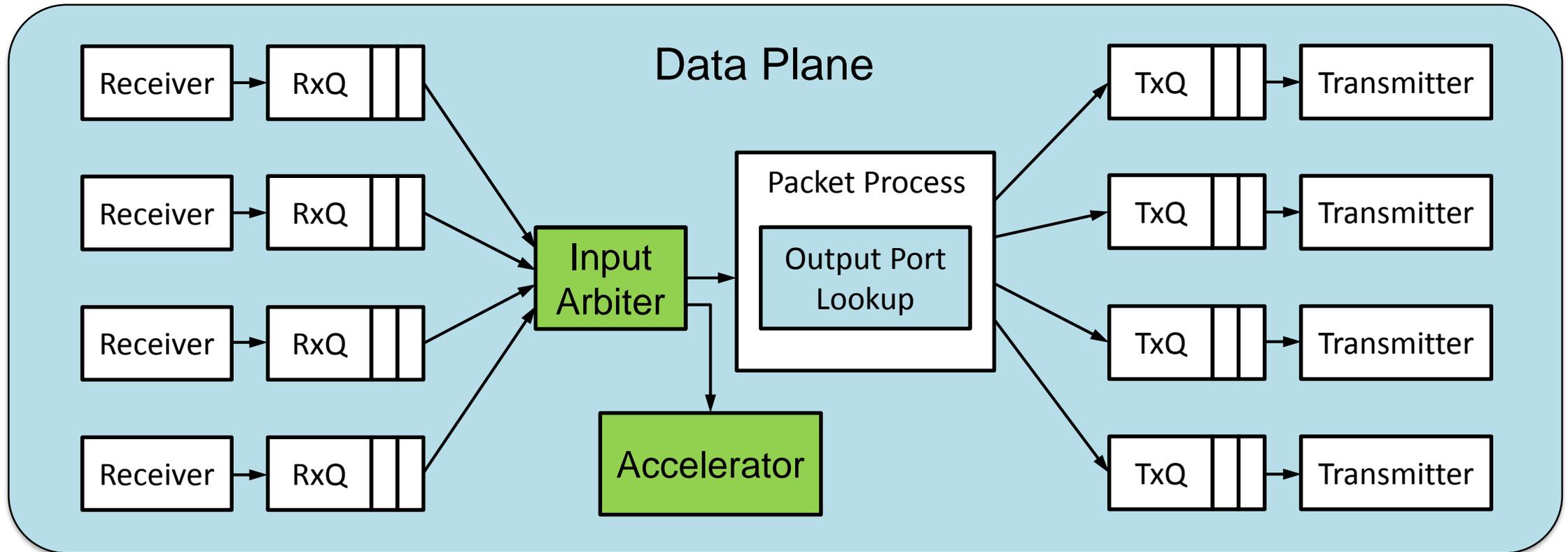
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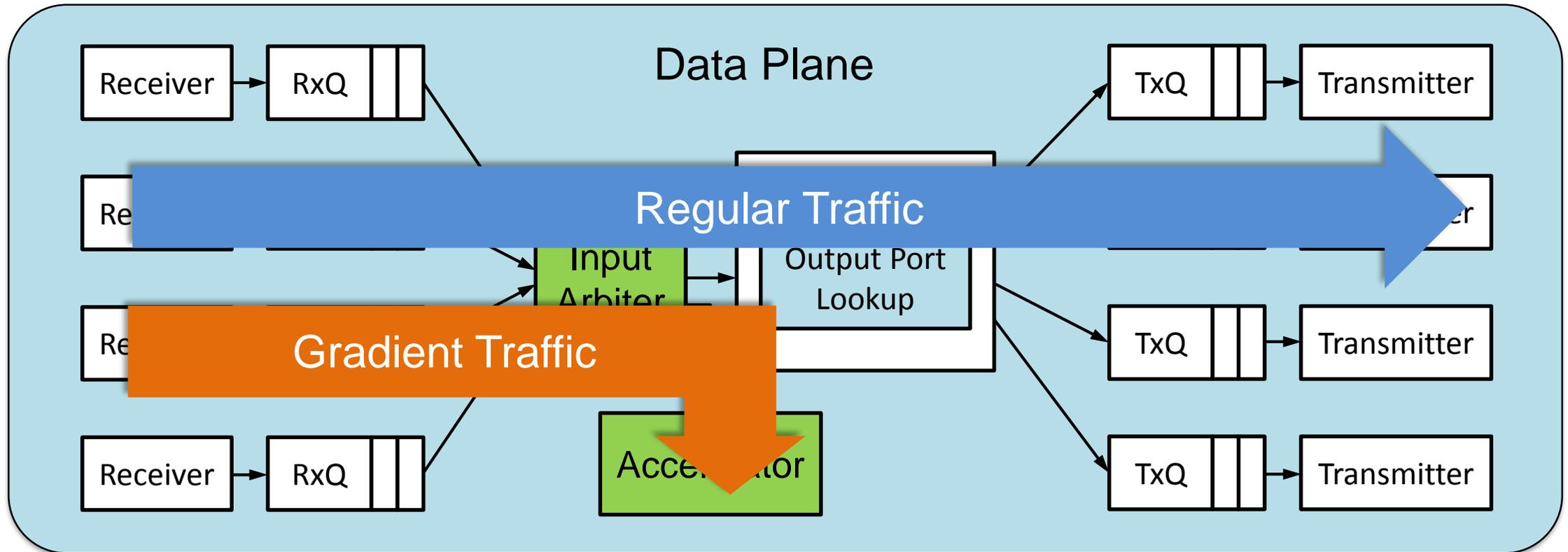
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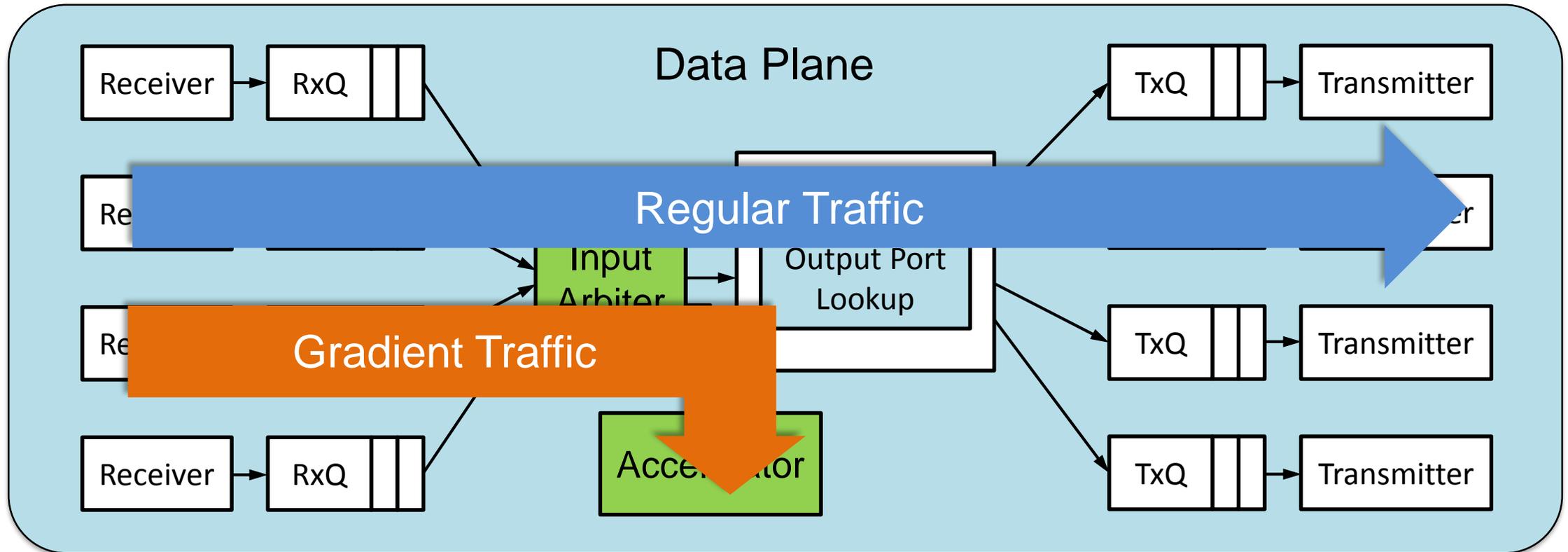
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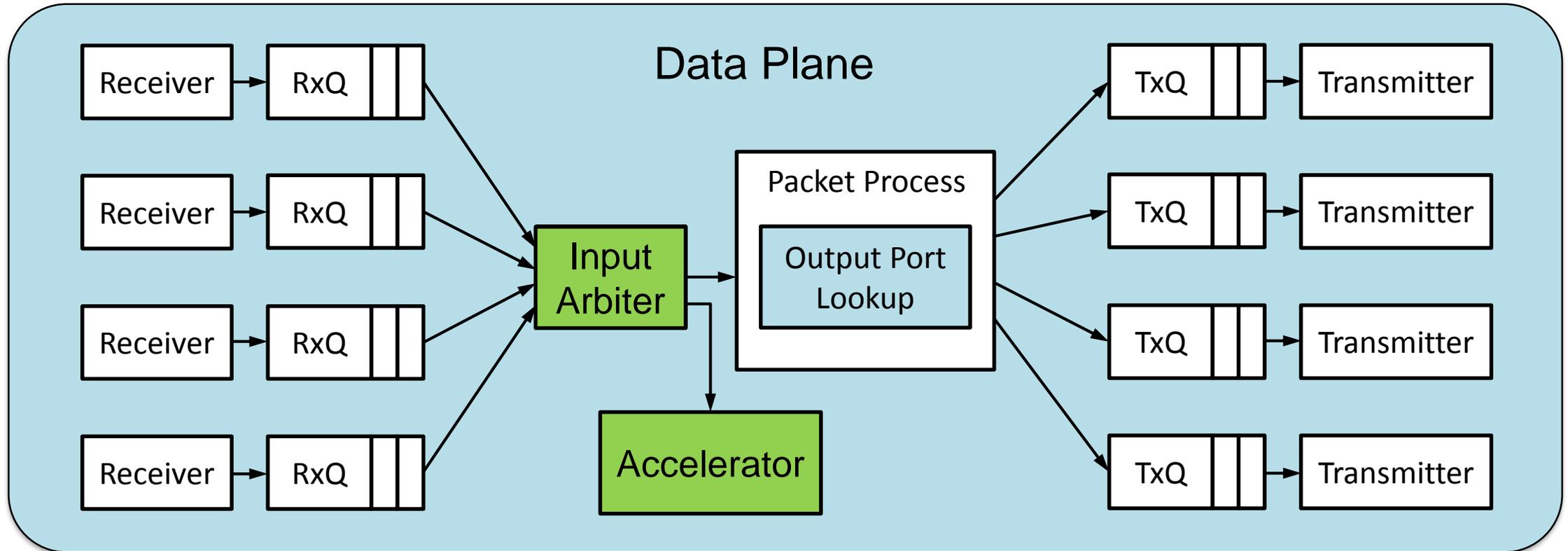


Integrating Aggregation Accelerator into the Programmable Switch



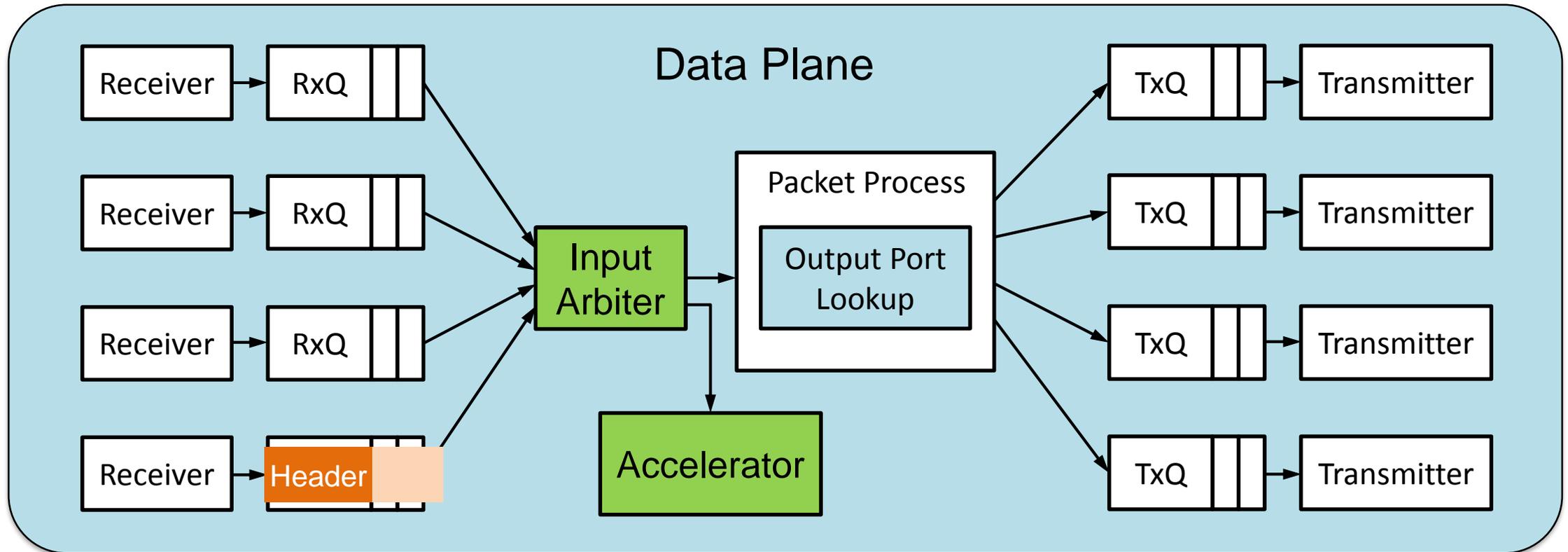
Hardware Acceleration Isolated From Regular Switch Function

Integrating Aggregation Accelerator into the Programmable Switch



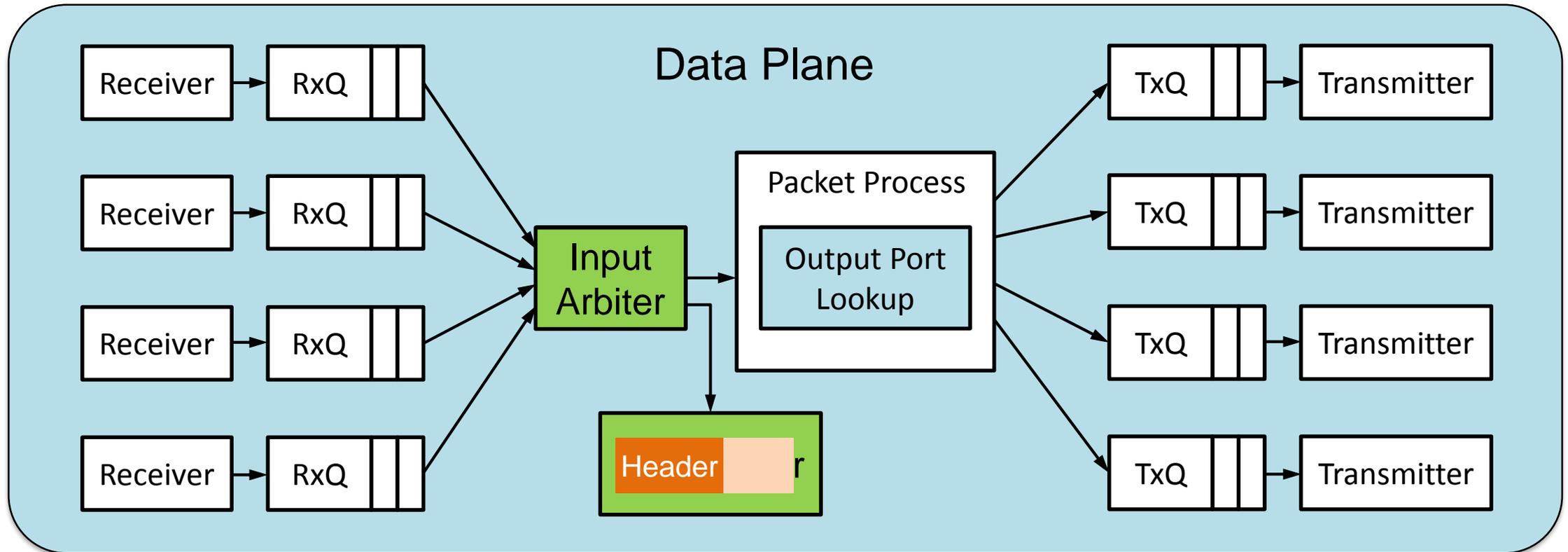
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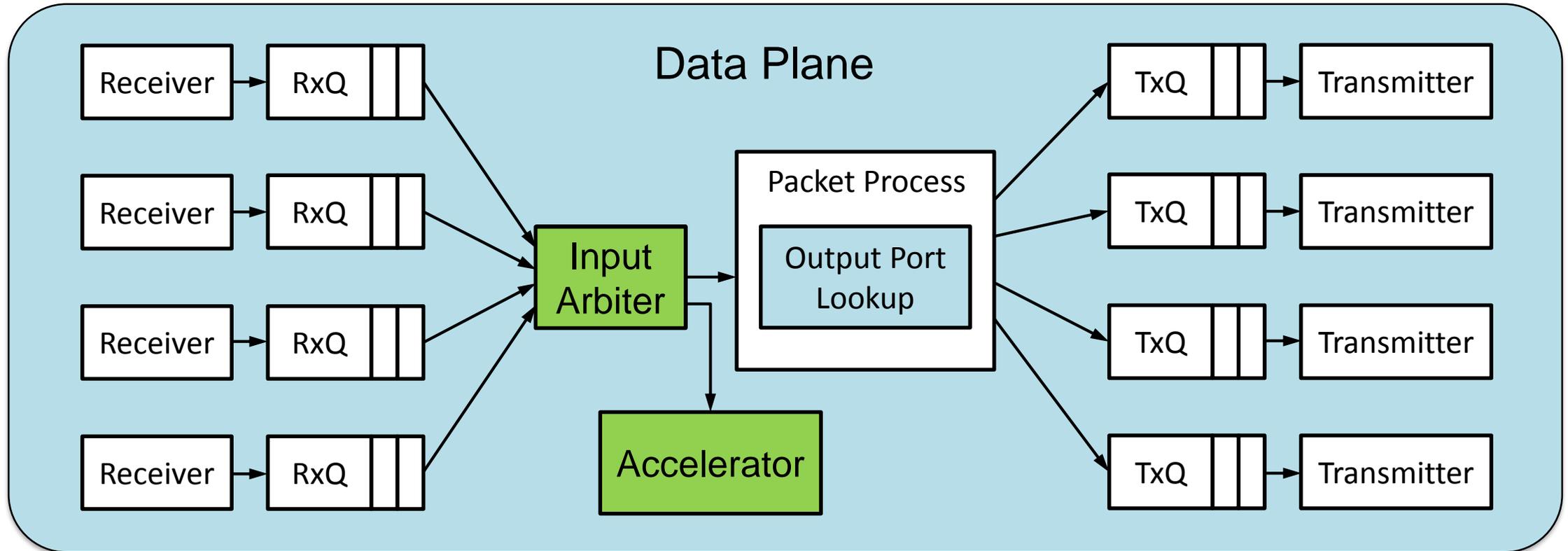
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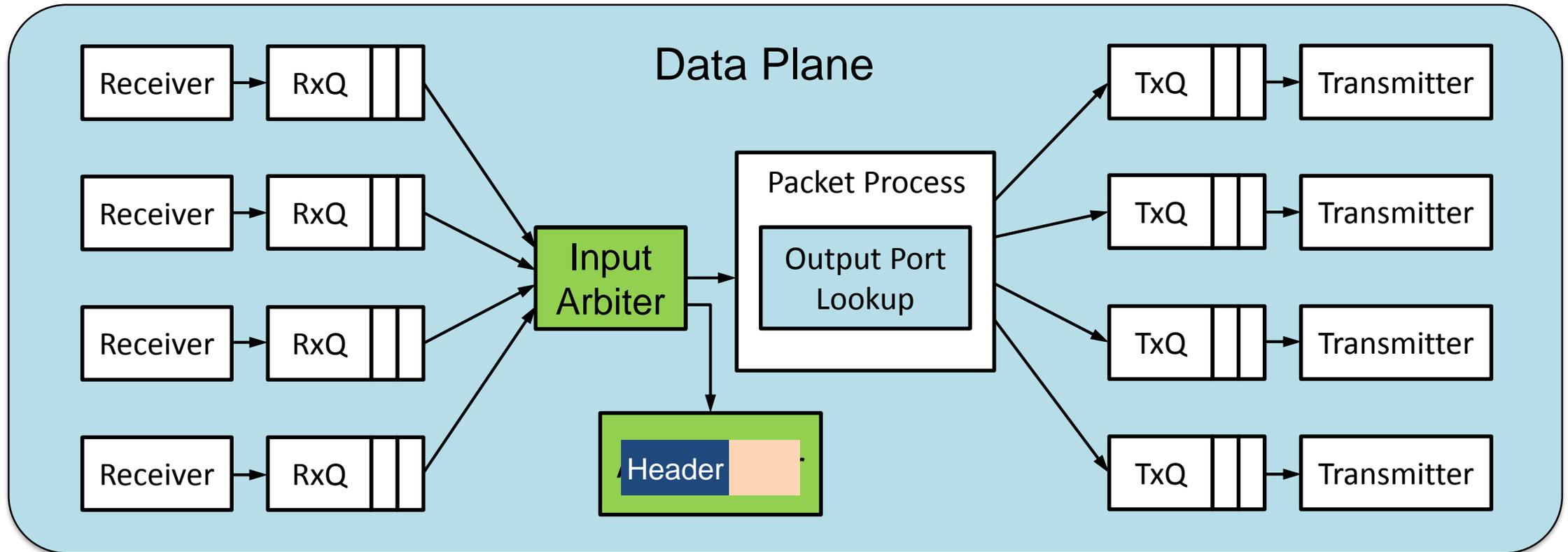
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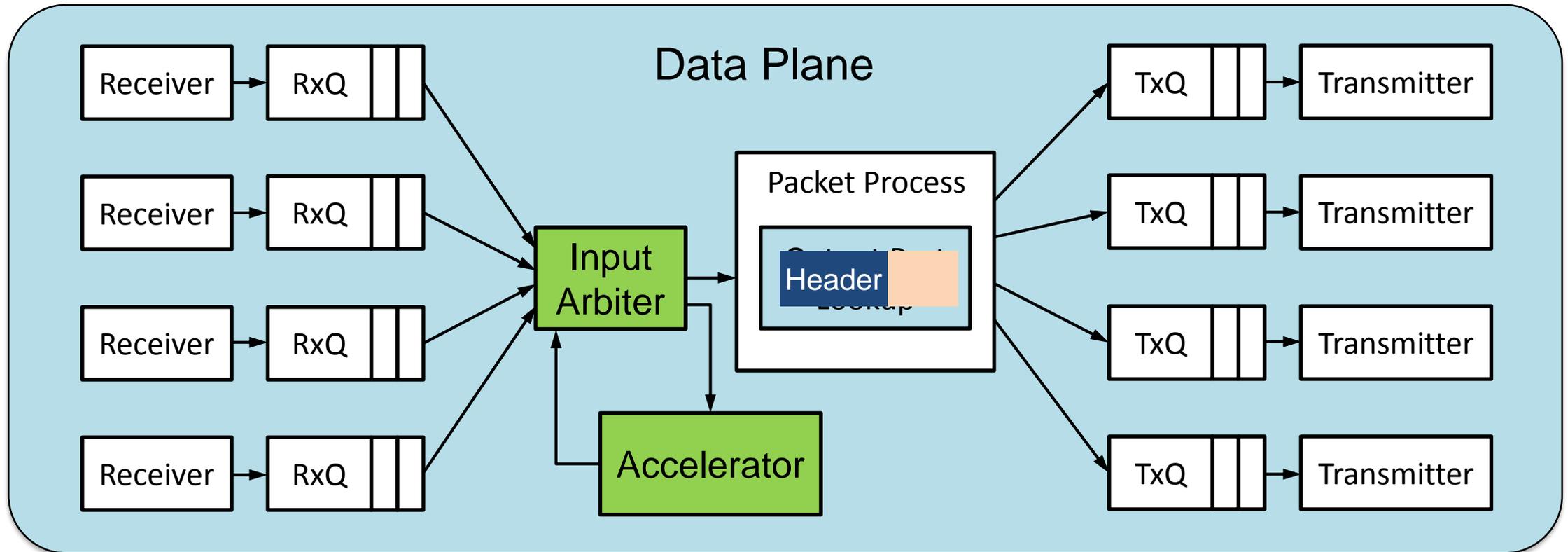
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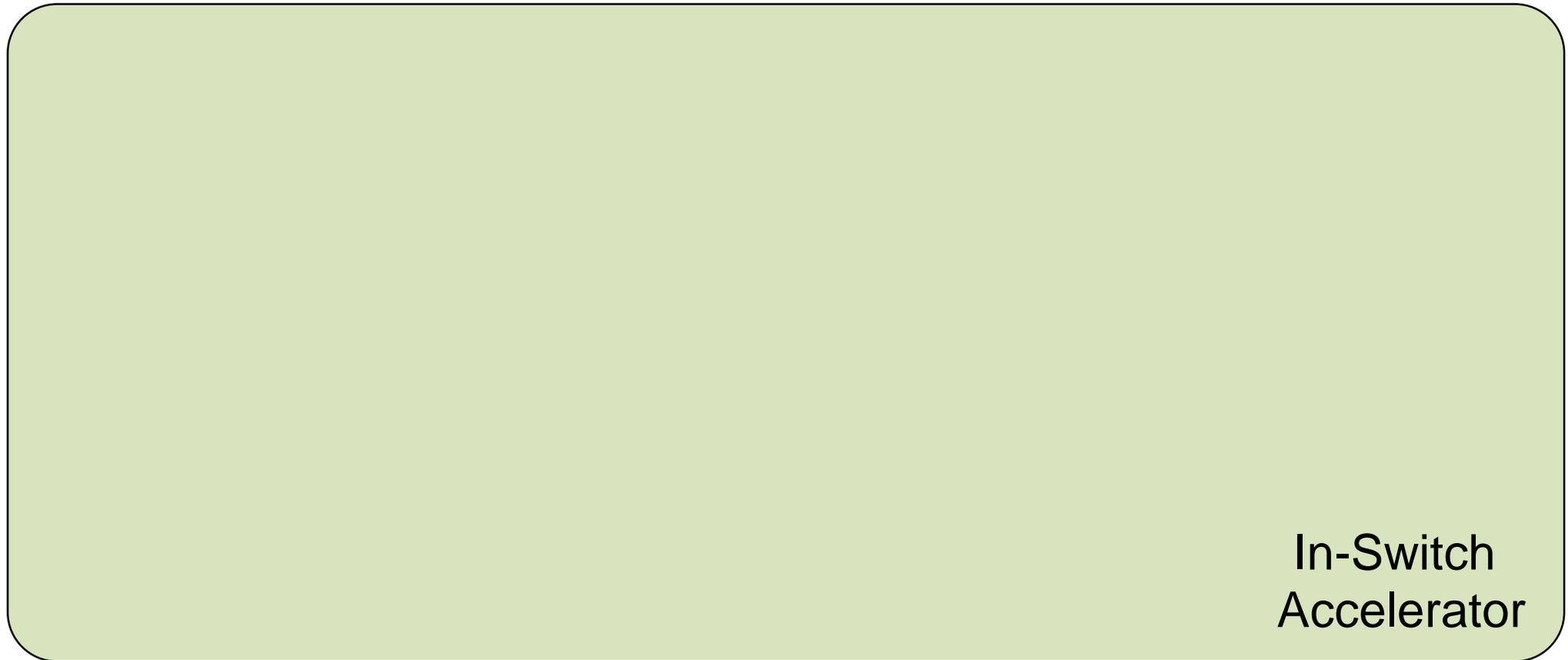
Hardware Acceleration Isolated From Regular Switch Function

Integrating Aggregation Accelerator into the Programmable Switch



Hardware Acceleration Isolated From Regular Switch Function

Developing Light-Weight Accelerator for Aggregation



In-Switch
Accelerator

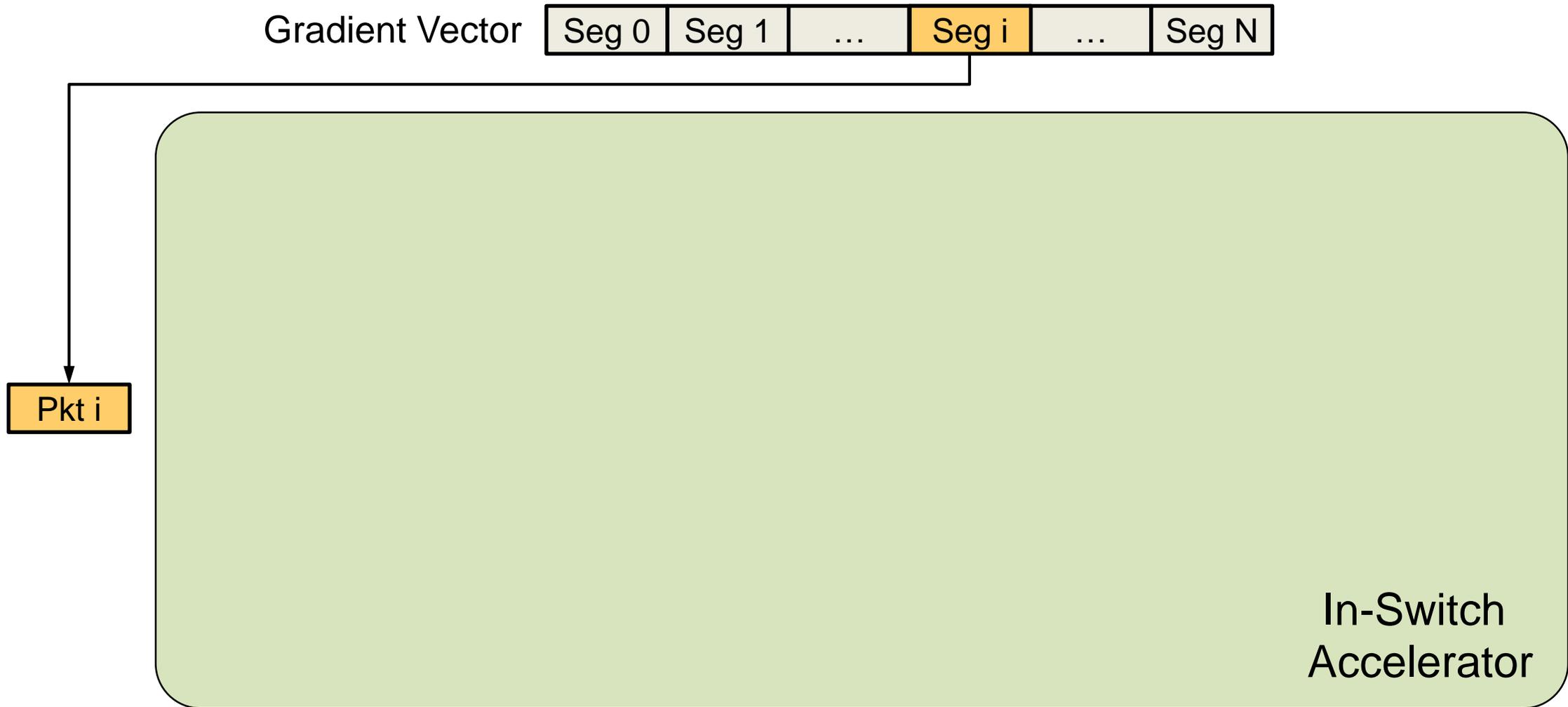
Developing Light-Weight Accelerator for Aggregation

Gradient Vector

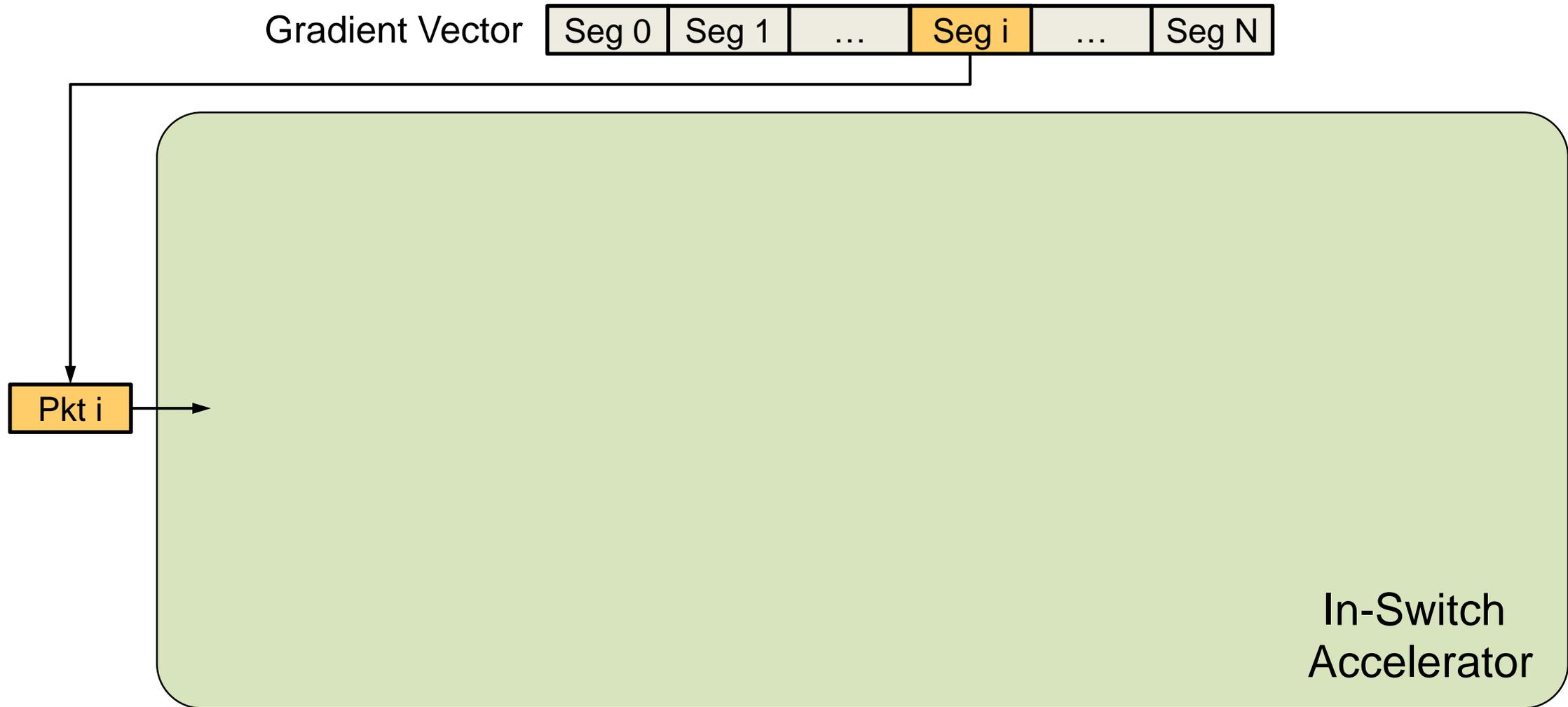
Seg 0	Seg 1	...	Seg i	...	Seg N
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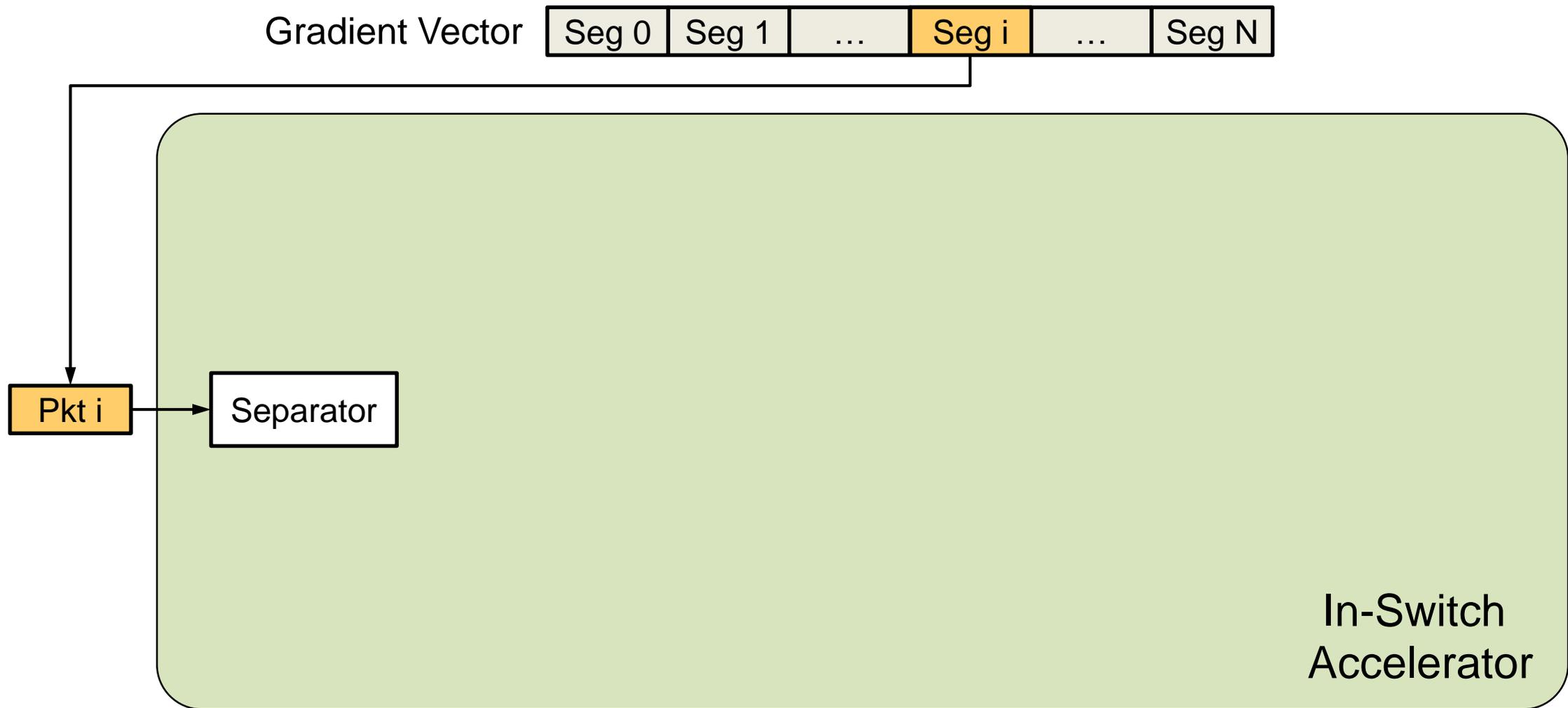
Developing Light-Weight Accelerator for Aggregation



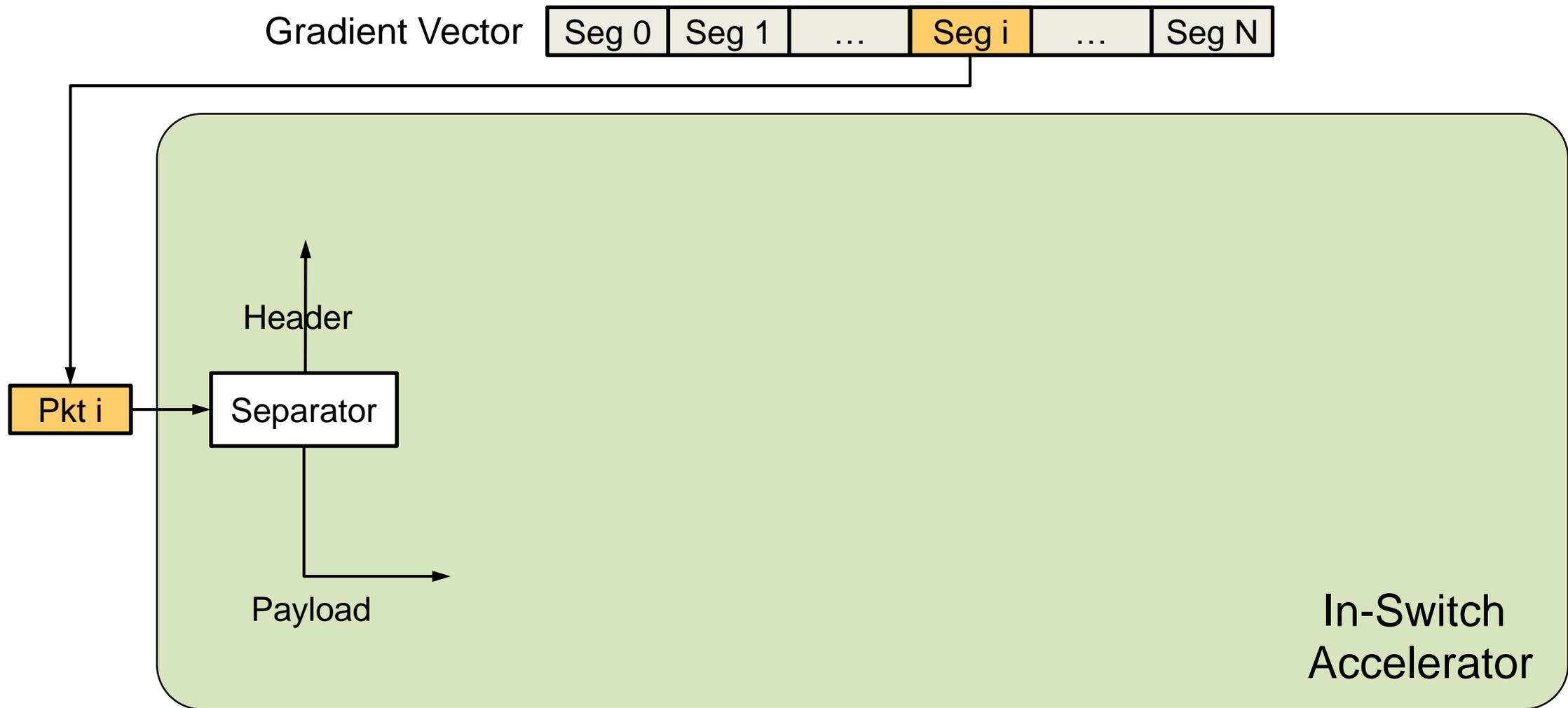
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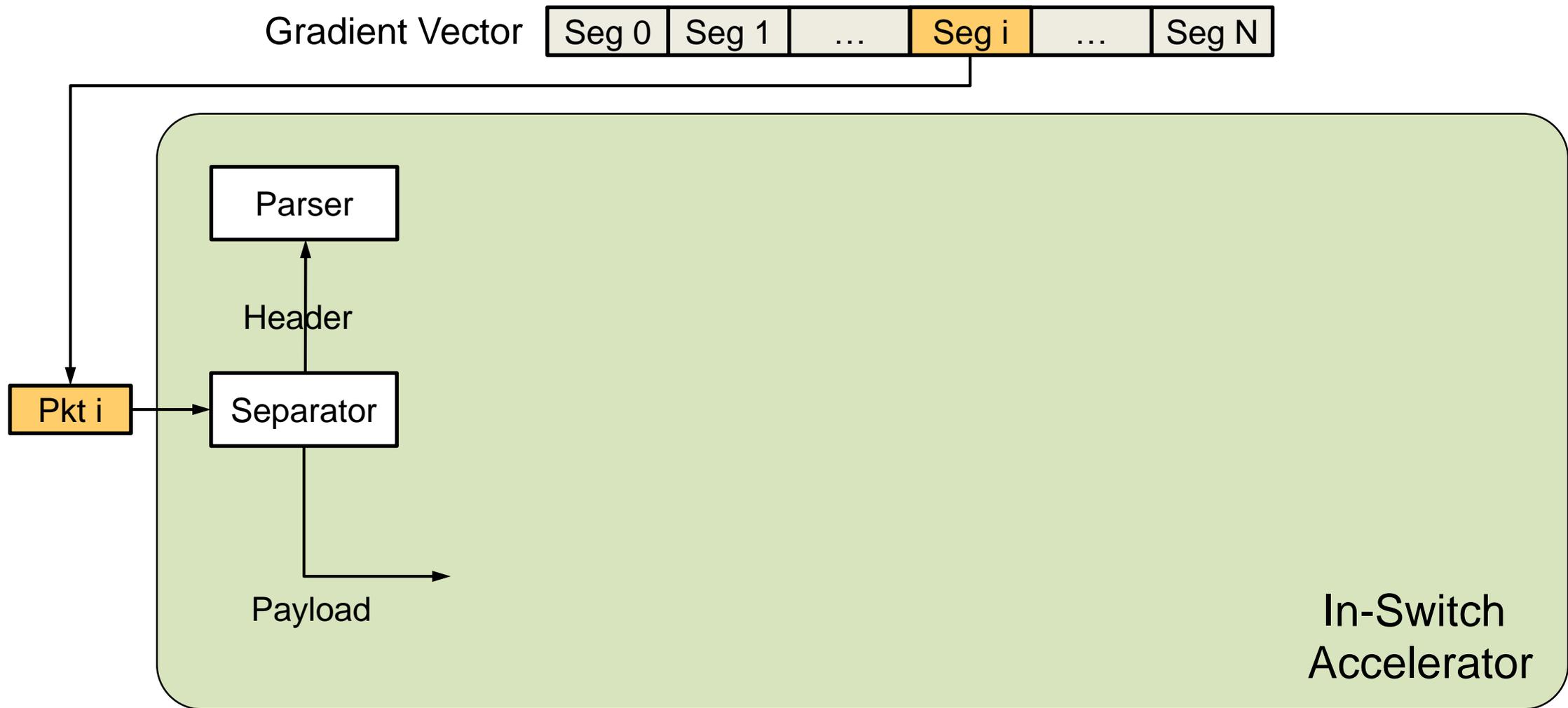
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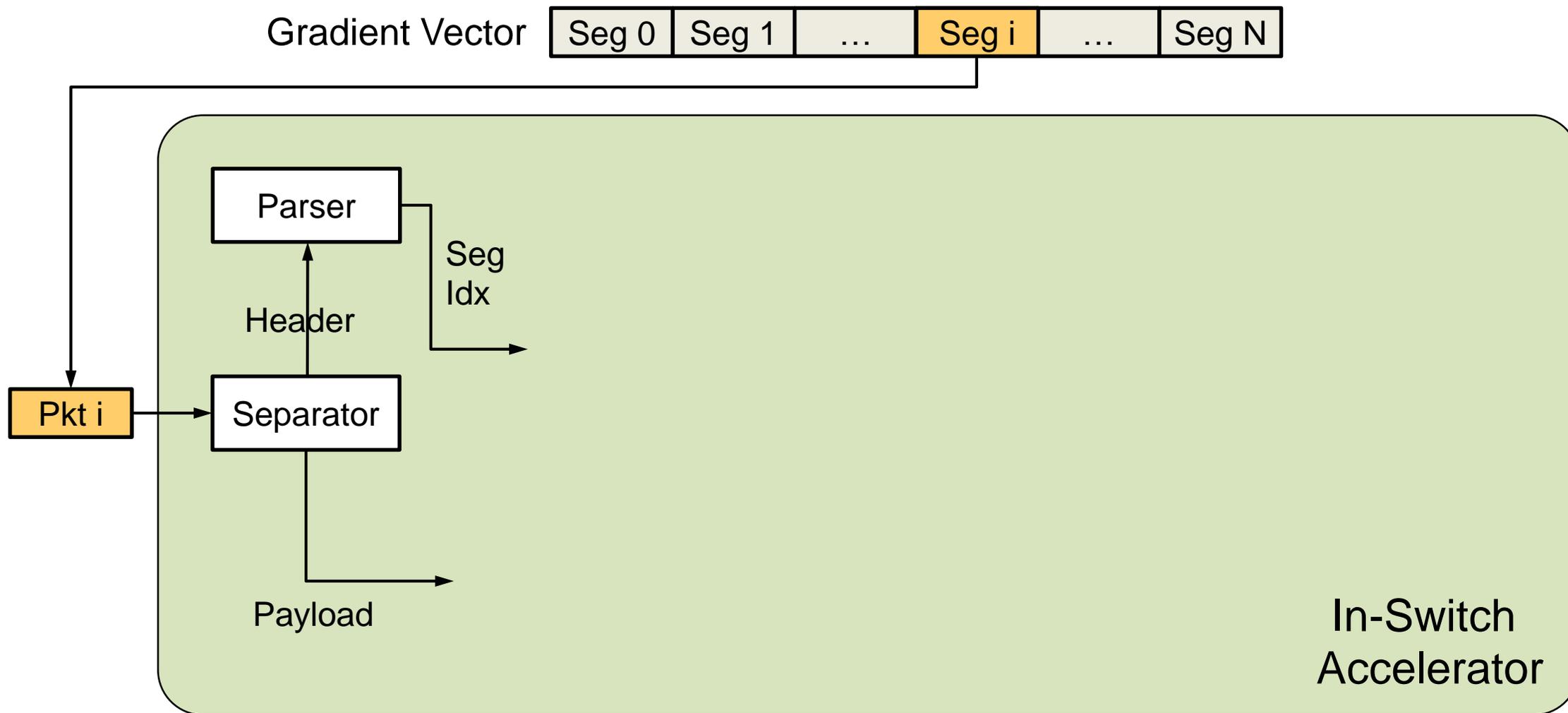
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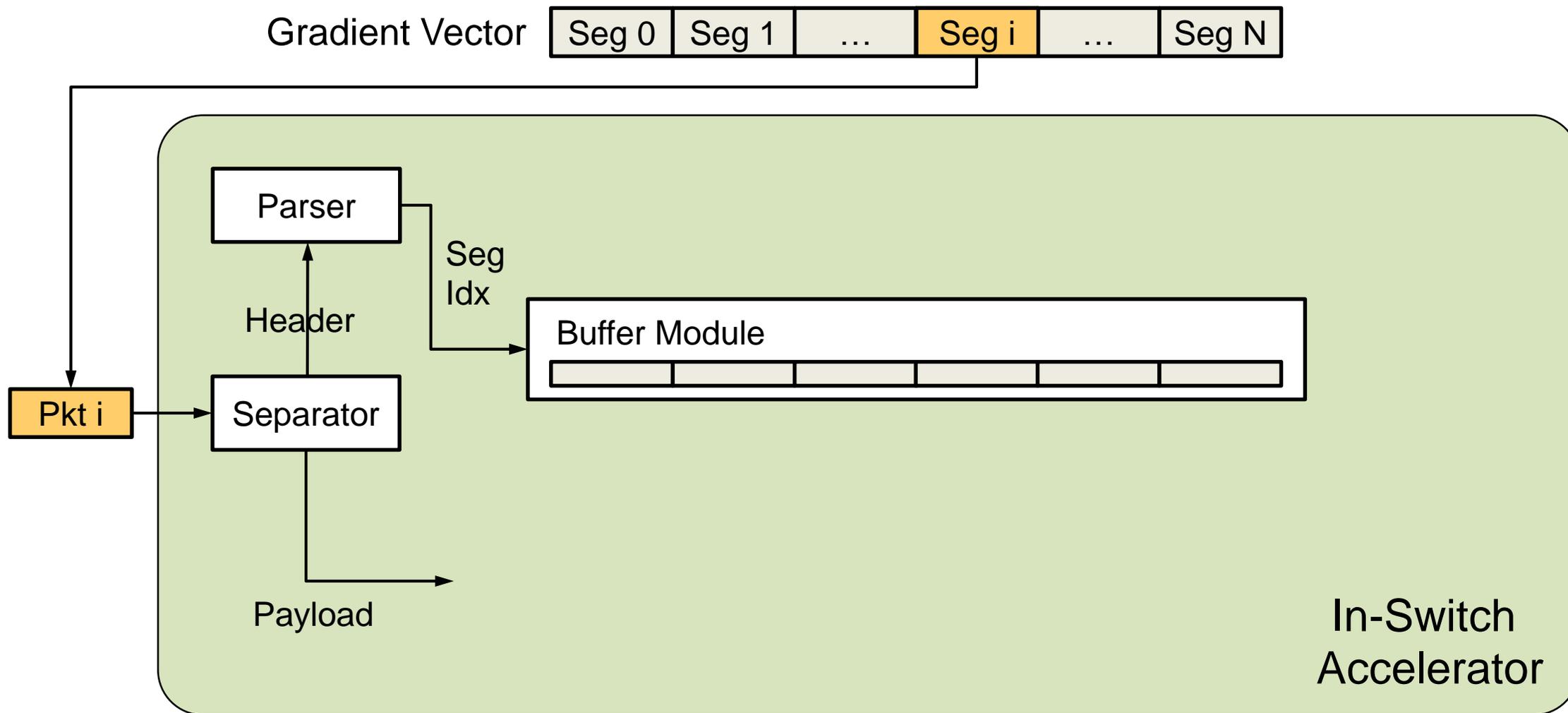
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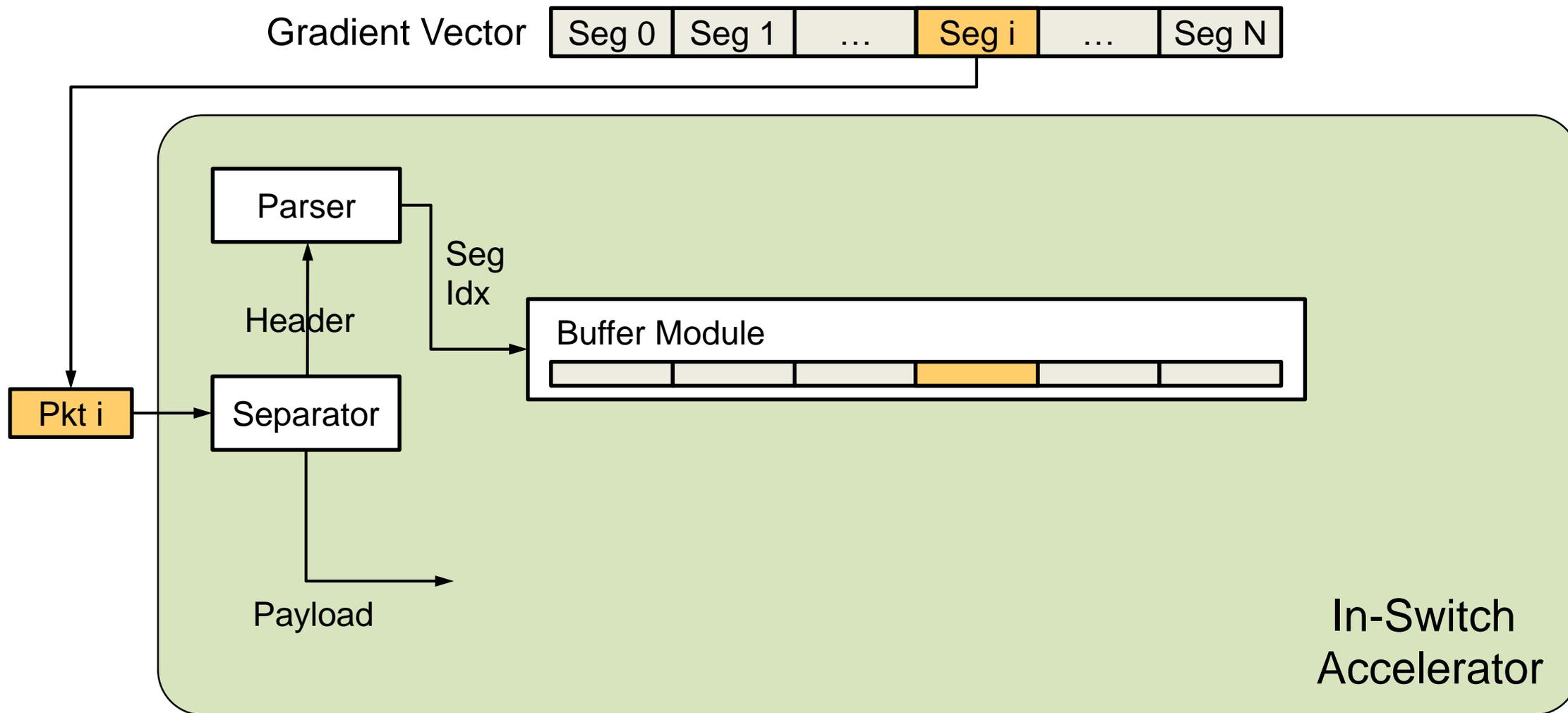
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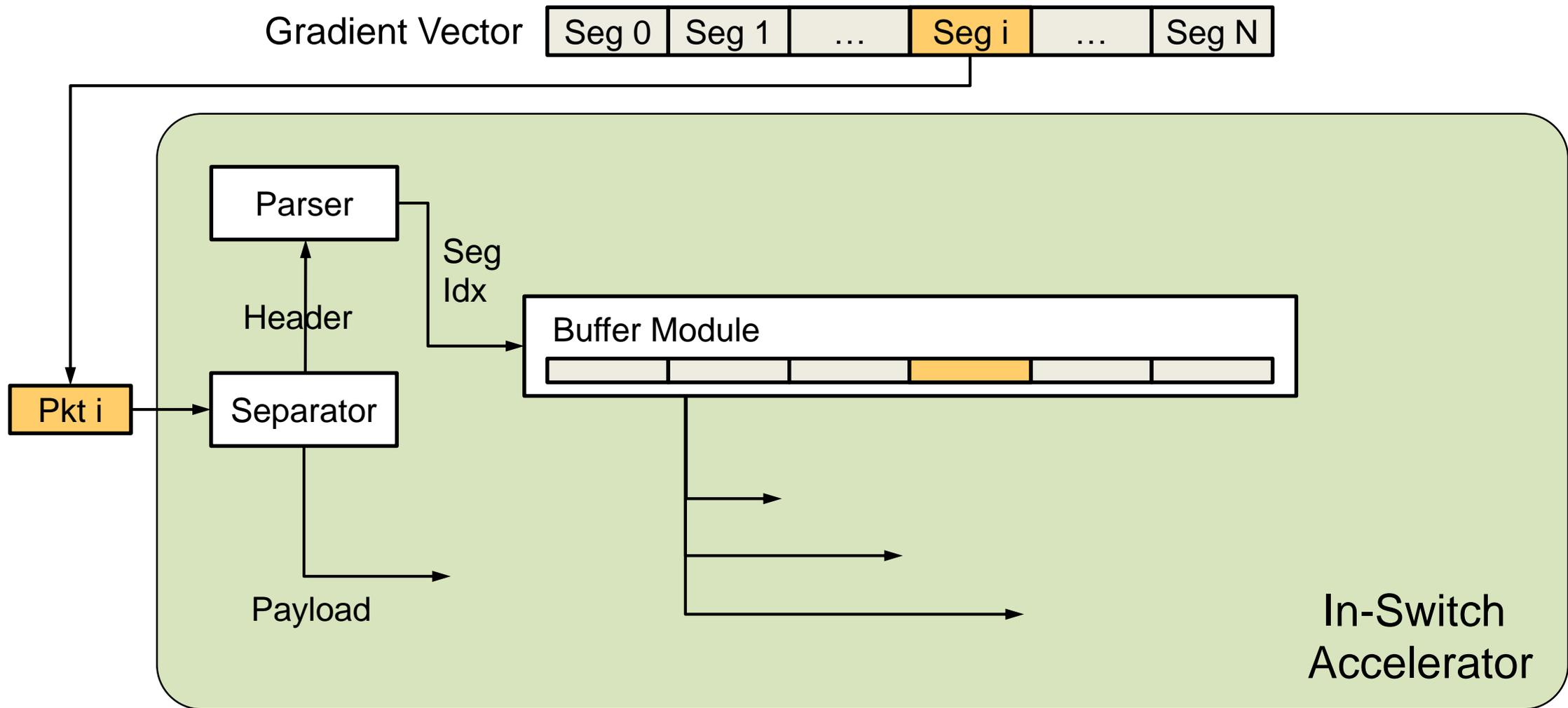
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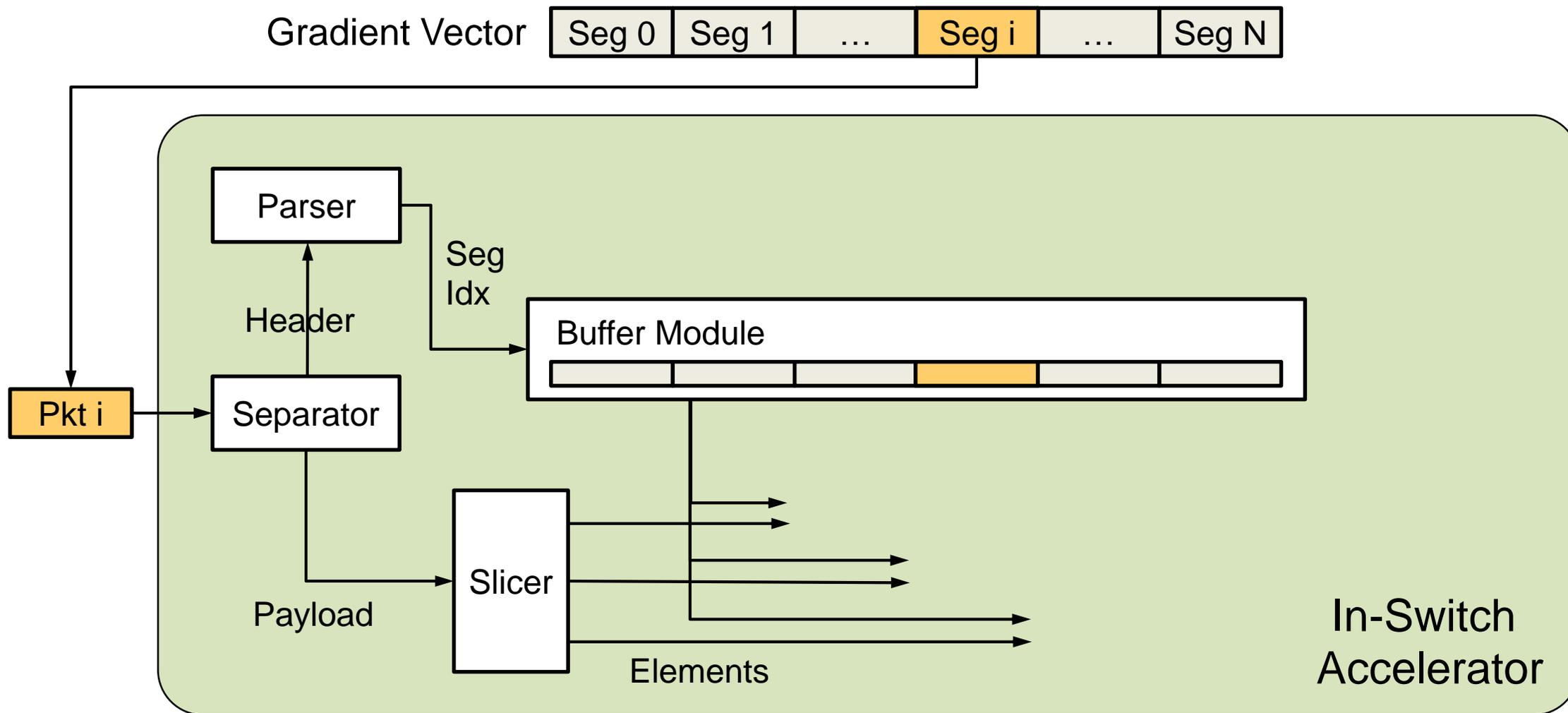
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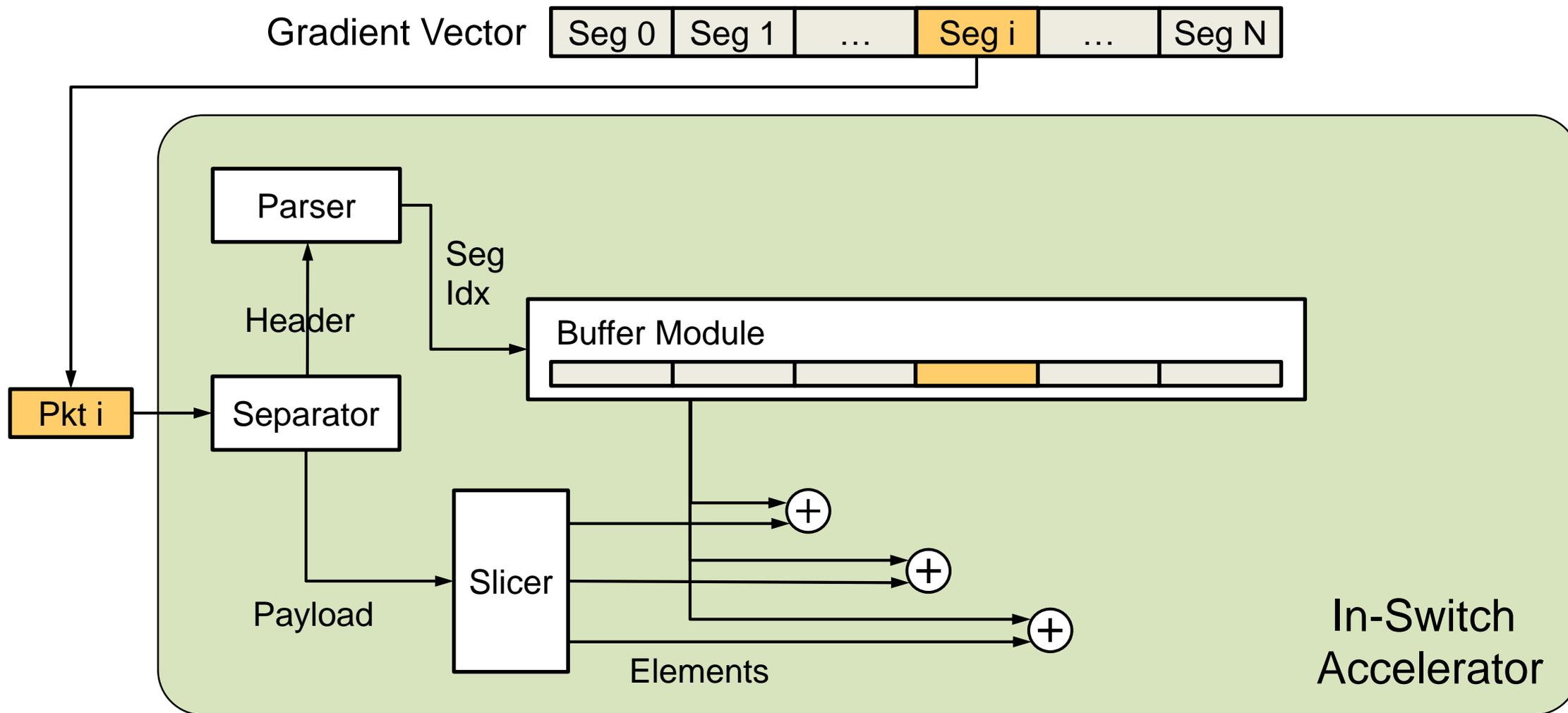
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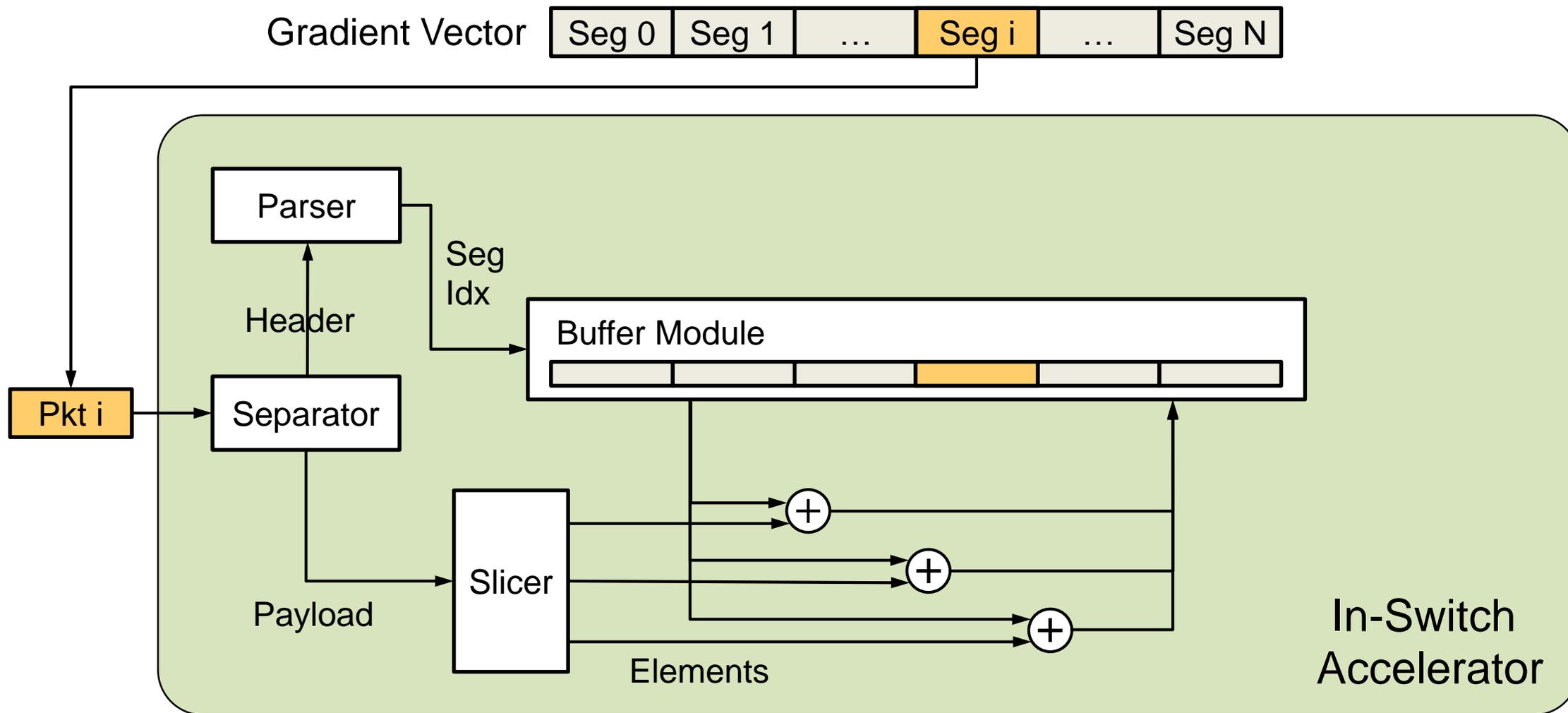
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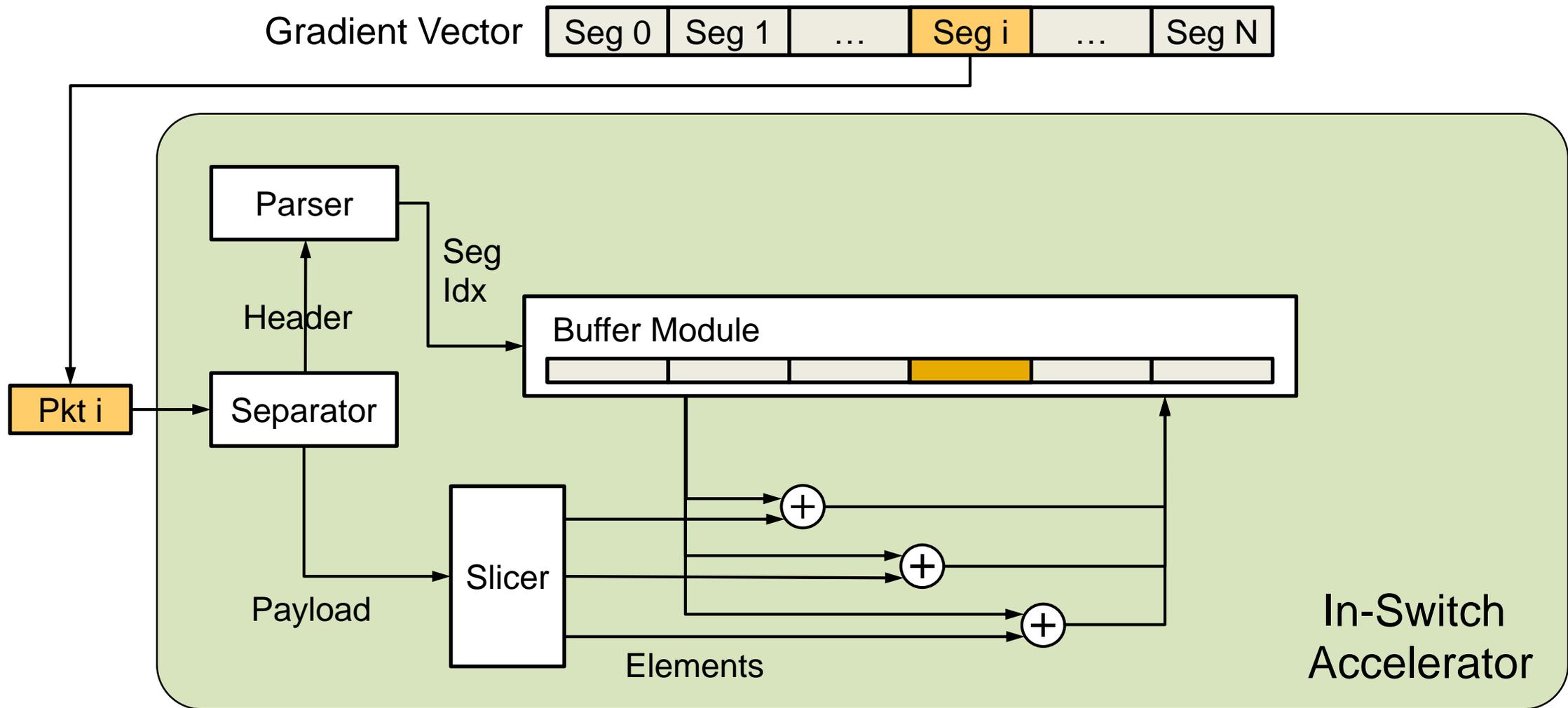
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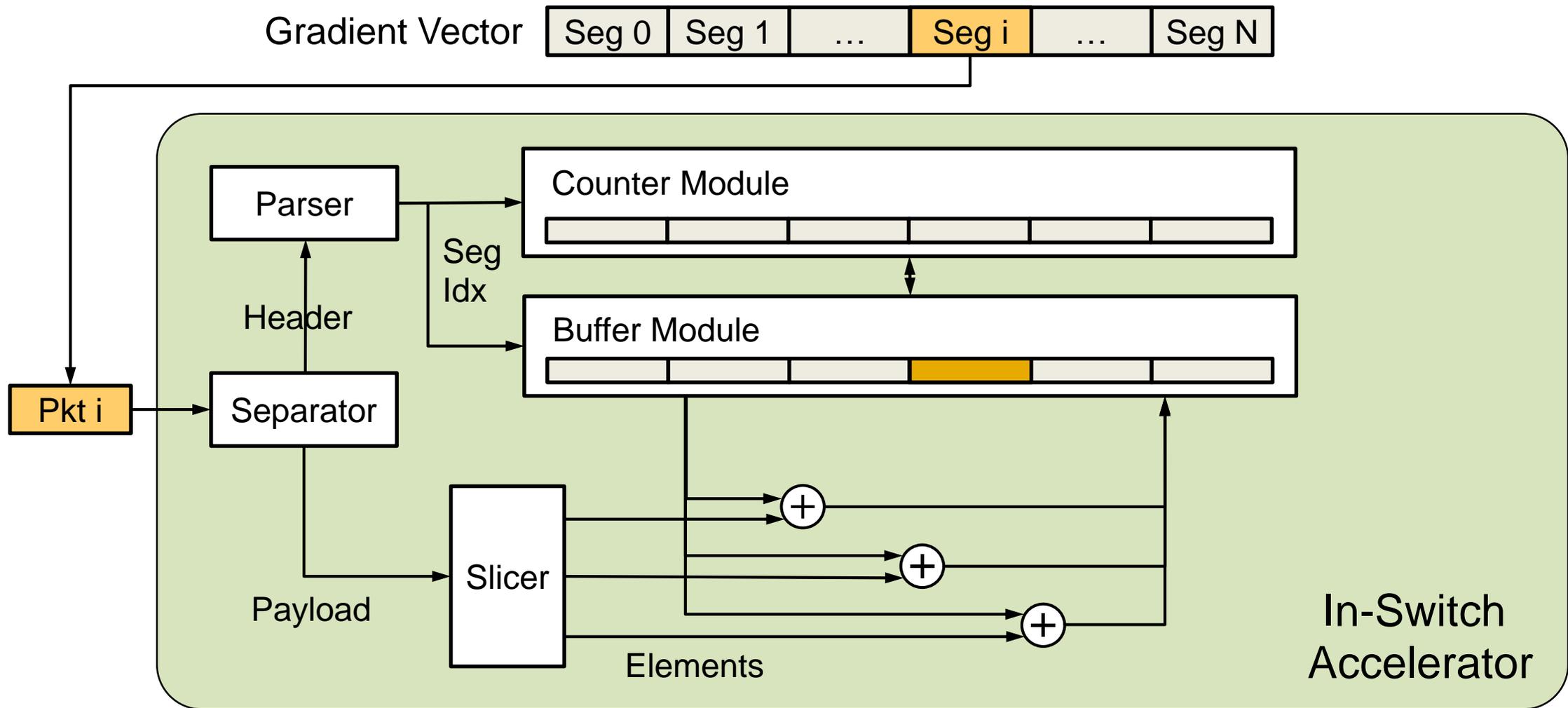
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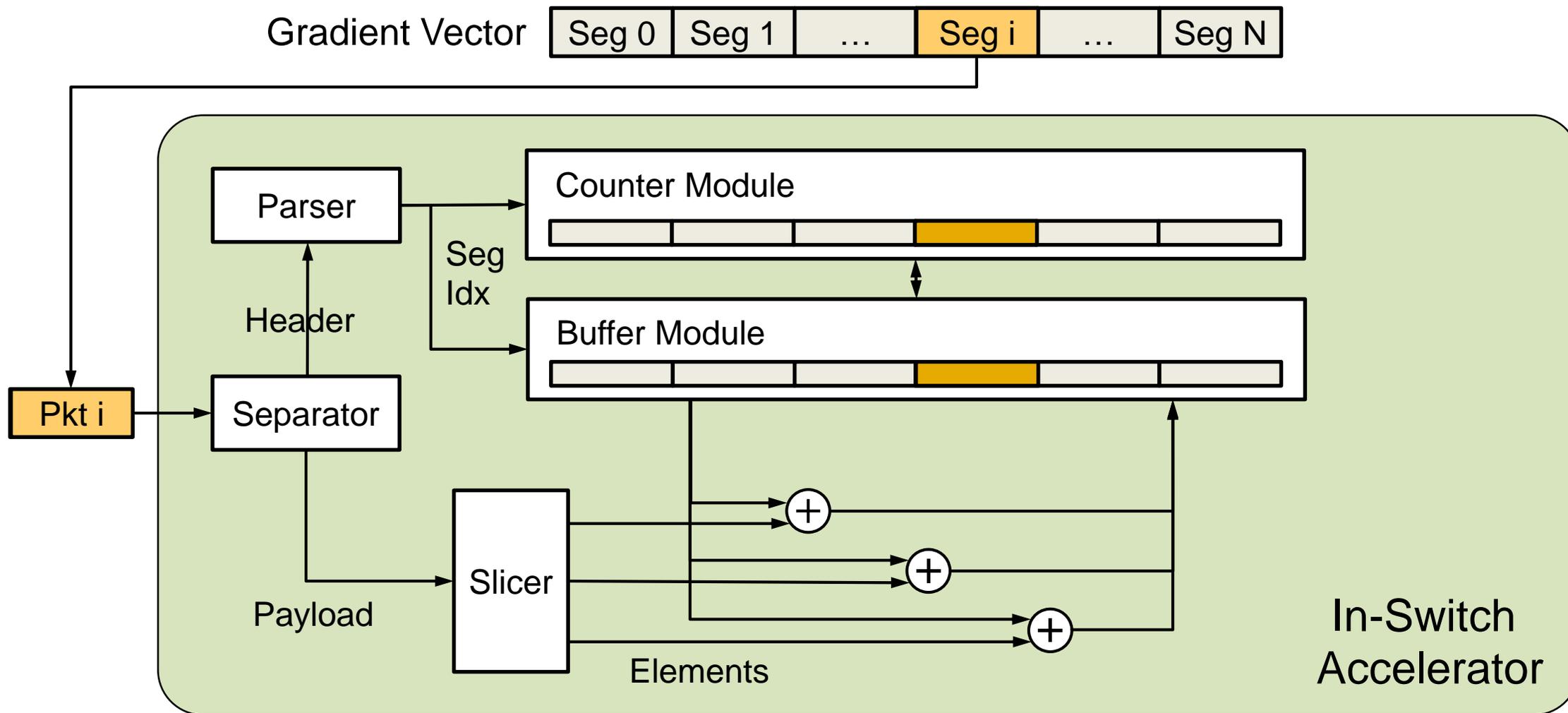
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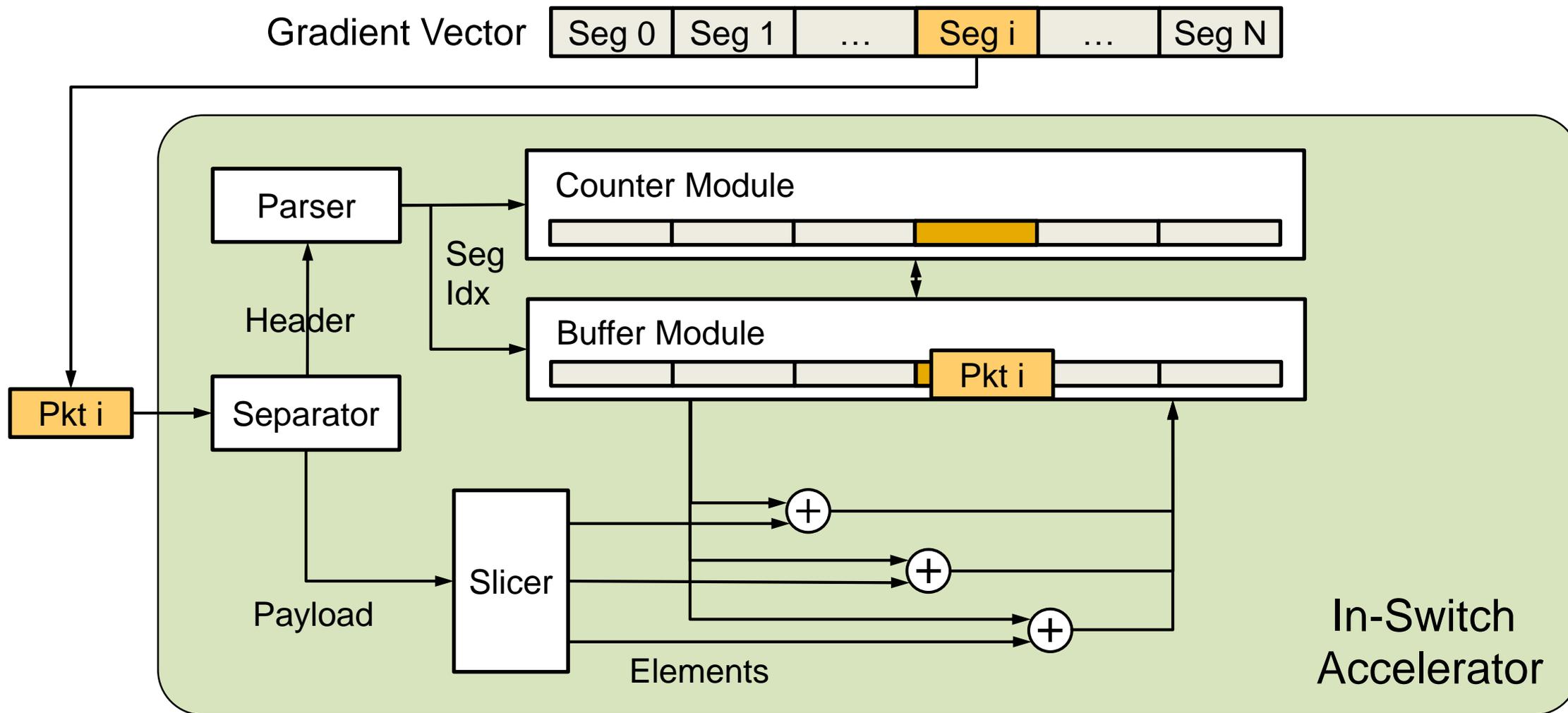
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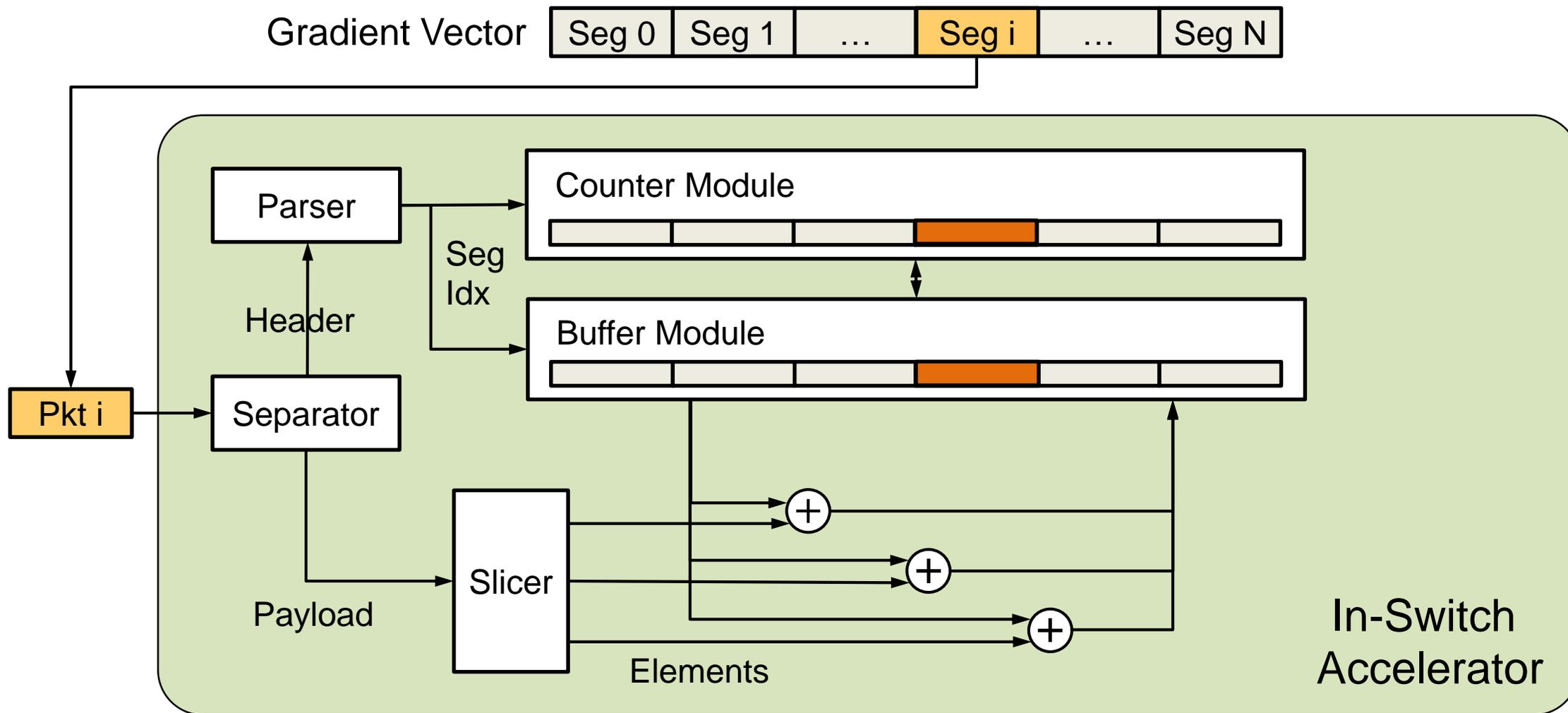
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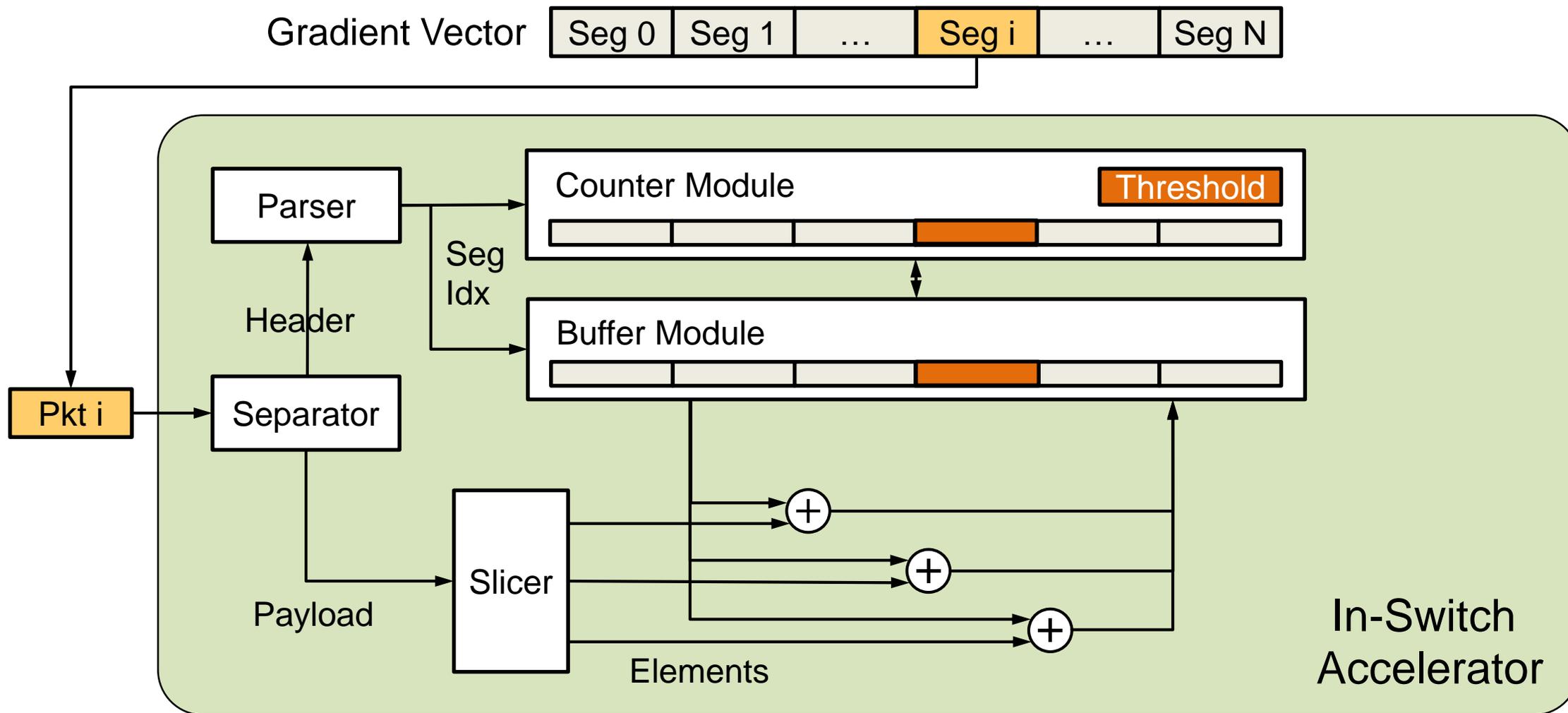
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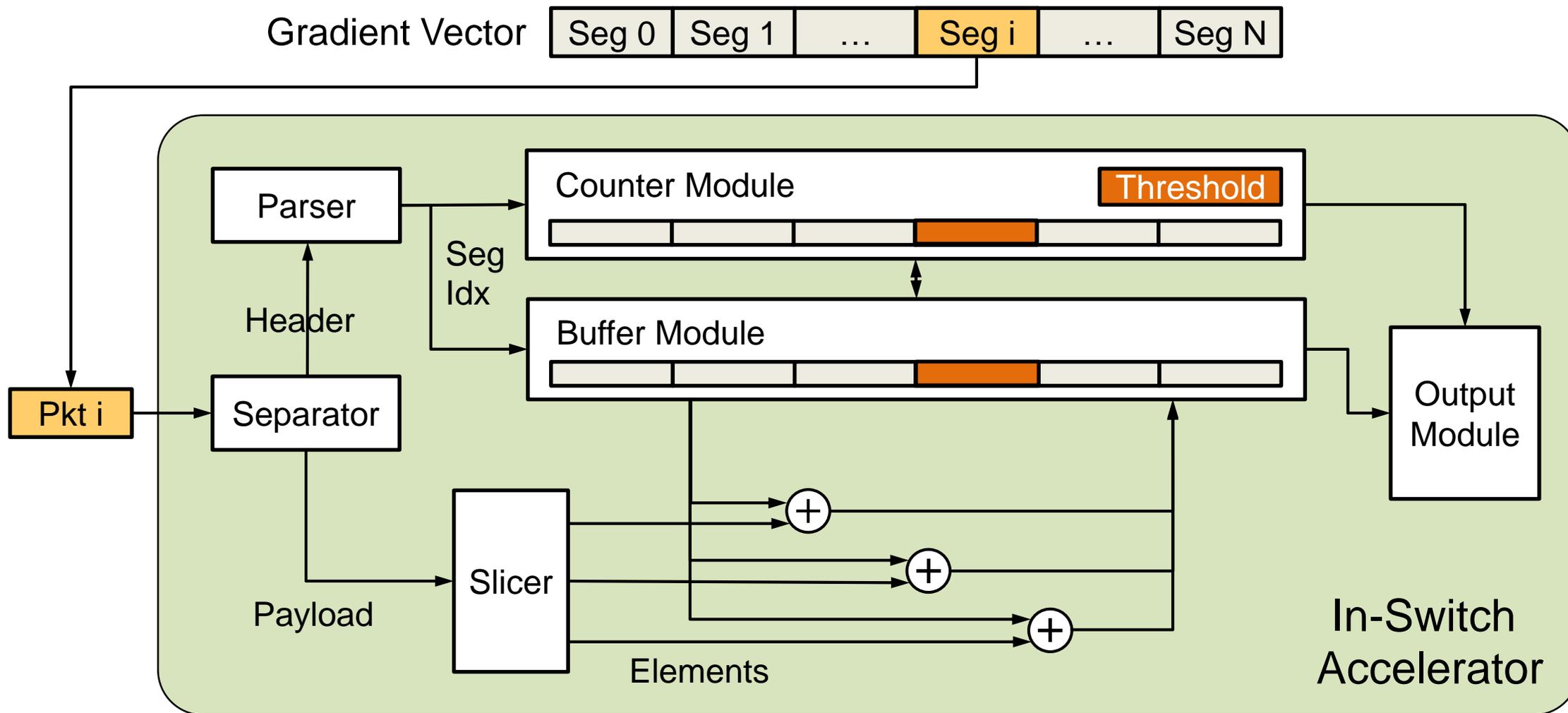
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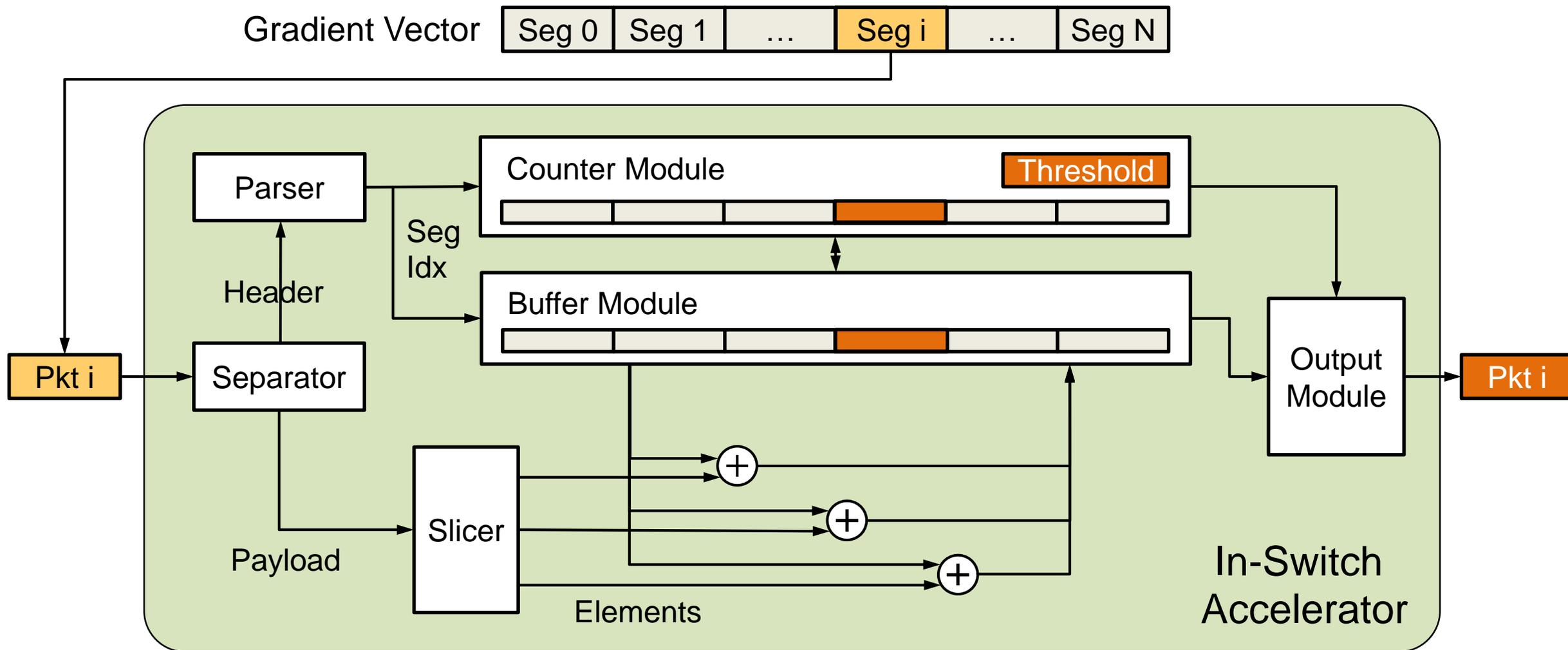
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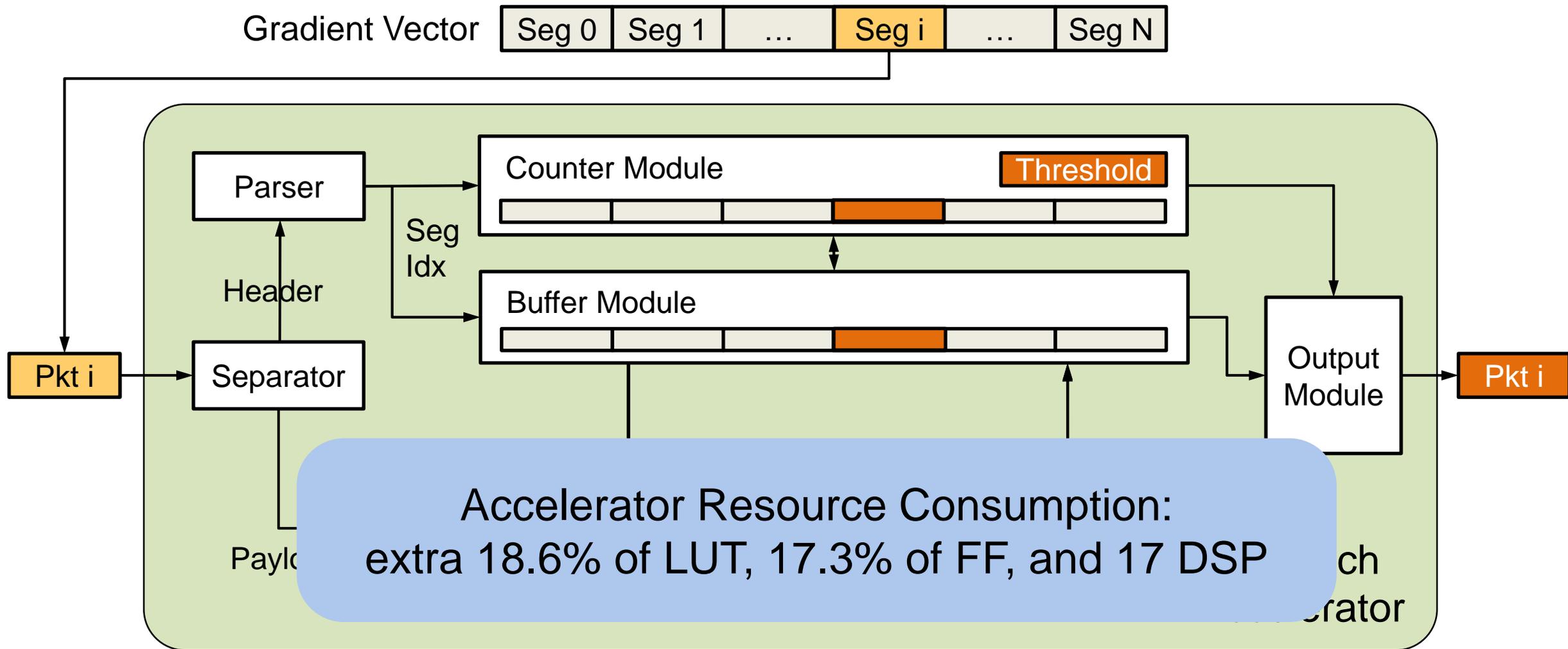
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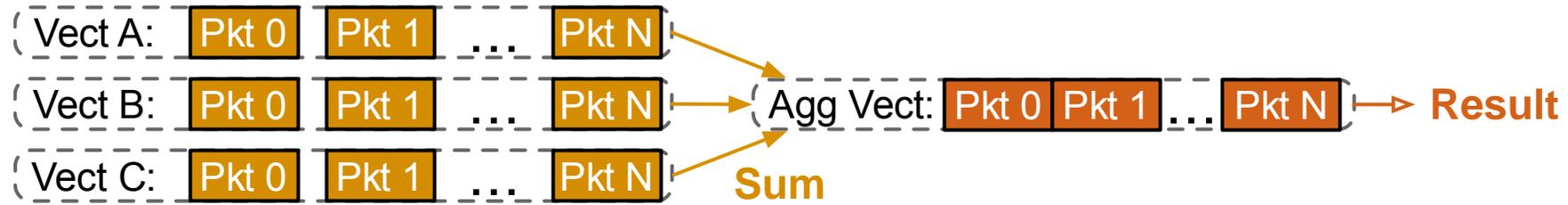
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Developing Light-Weight Accelerator for Aggregation

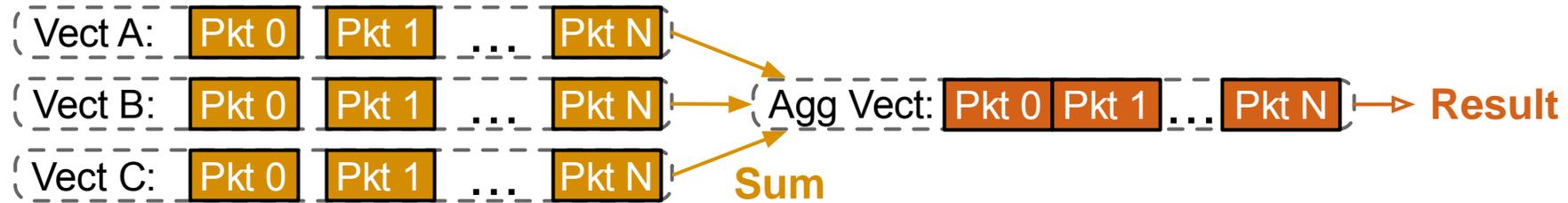


Aggregating Gradient at Packet-Level for Improved Parallelism

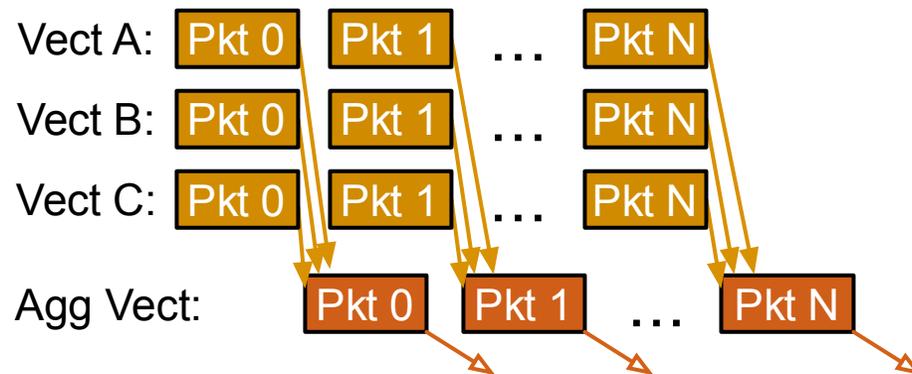


Conventional Vector-Level Aggregation

Aggregating Gradient at Packet-Level for Improved Parallelism

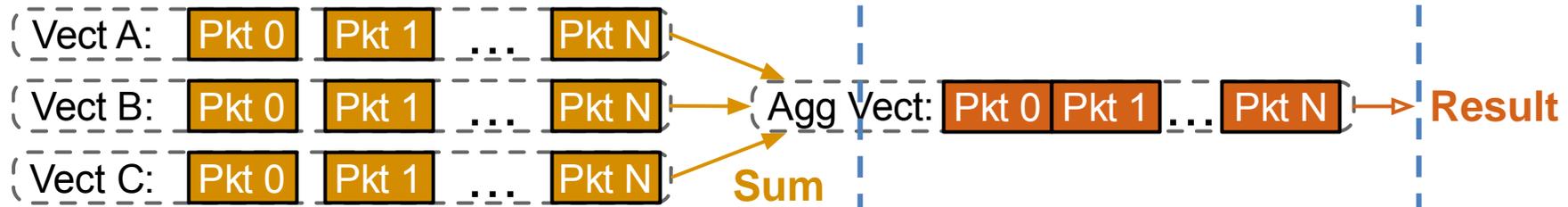


Conventional Vector-Level Aggregation

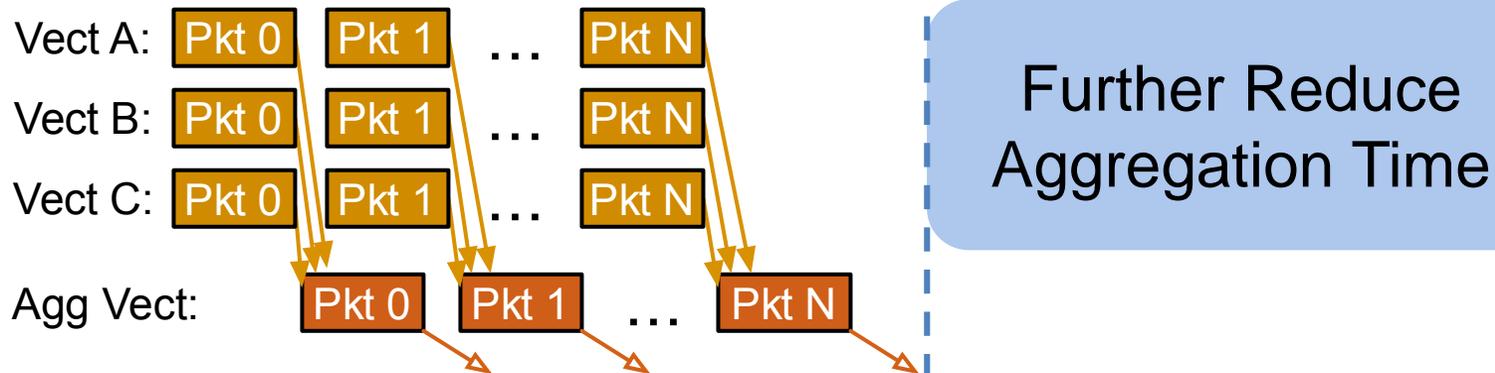


Packet-Level Aggregation in Our iSwitch

Aggregating Gradient at Packet-Level for Improved Parallelism



Conventional Vector-Level Aggregation



Packet-Level Aggregation in Our iSwitch

Extending Network Protocol for In-Switch Computing

Regular Packet:



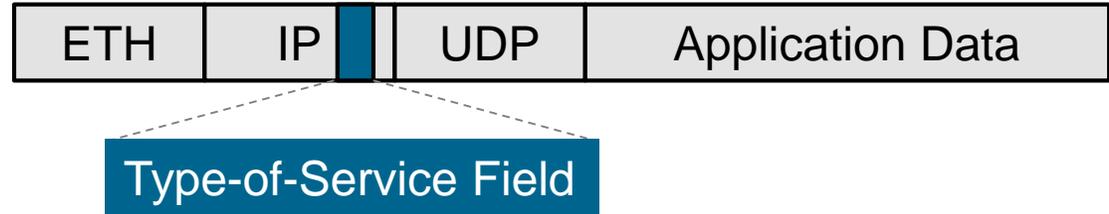
Extending Network Protocol for In-Switch Computing

Data Packet of iSwitch:



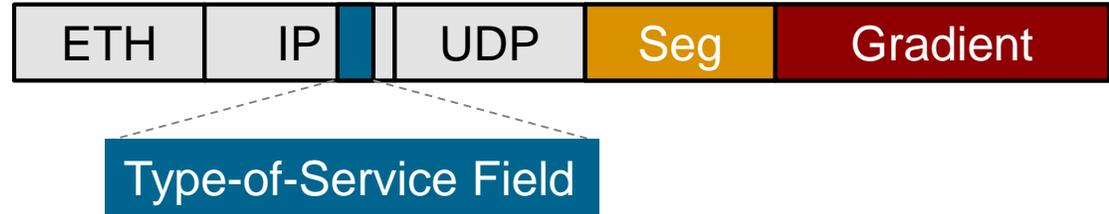
Extending Network Protocol for In-Switch Computing

Data Packet of iSwitch:



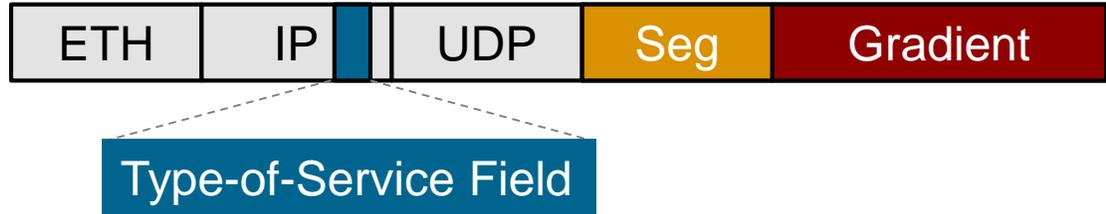
Extending Network Protocol for In-Switch Computing

Data Packet of iSwitch:



Extending Network Protocol for In-Switch Computing

Data Packet of iSwitch:



Control Packet of iSwitch:



Extending Network Protocol for In-Switch Computing

Data Packet of iSwitch:



Type-of-Service Field

Control Packet of iSwitch:



Action	Description
Join	Join the training job
Leave	Leave the training job
Reset	Clear the accelerator on the switch
SetH	Set aggregation threshold H on switch
FBcast	Force broadcast a segment on switch
Help	Request a lost data packet for a worker
Ack	Confirm the success of some actions

Extending Network Protocol for In-Switch Computing

Data Packet of iSwitch:



Type-of-Service Field

Control Packet of iSwitch:

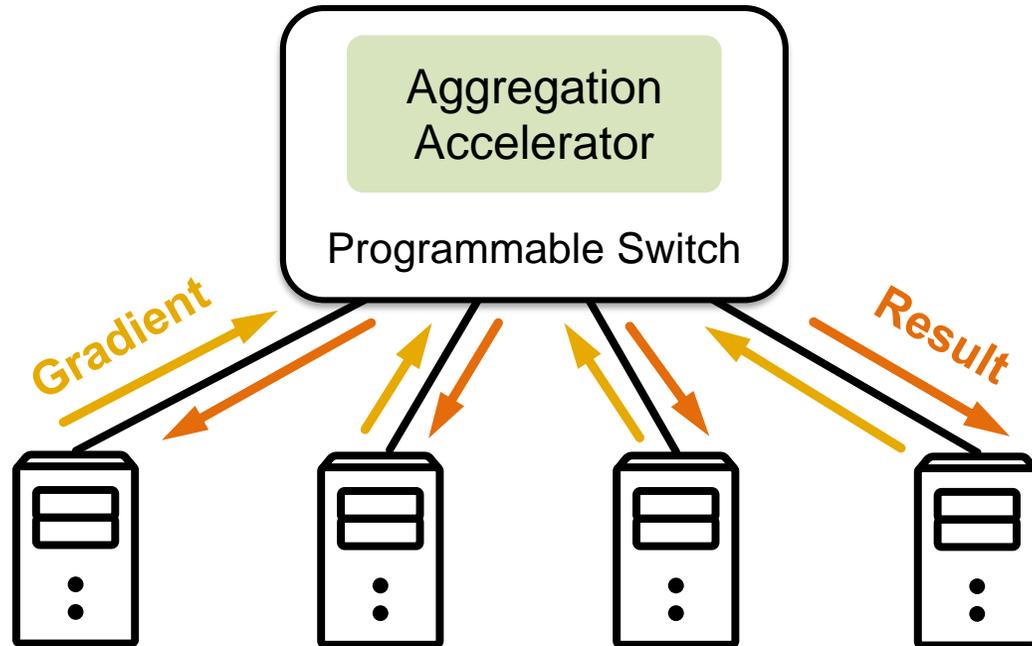


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iSwitch extension will NOT affect regular network functions

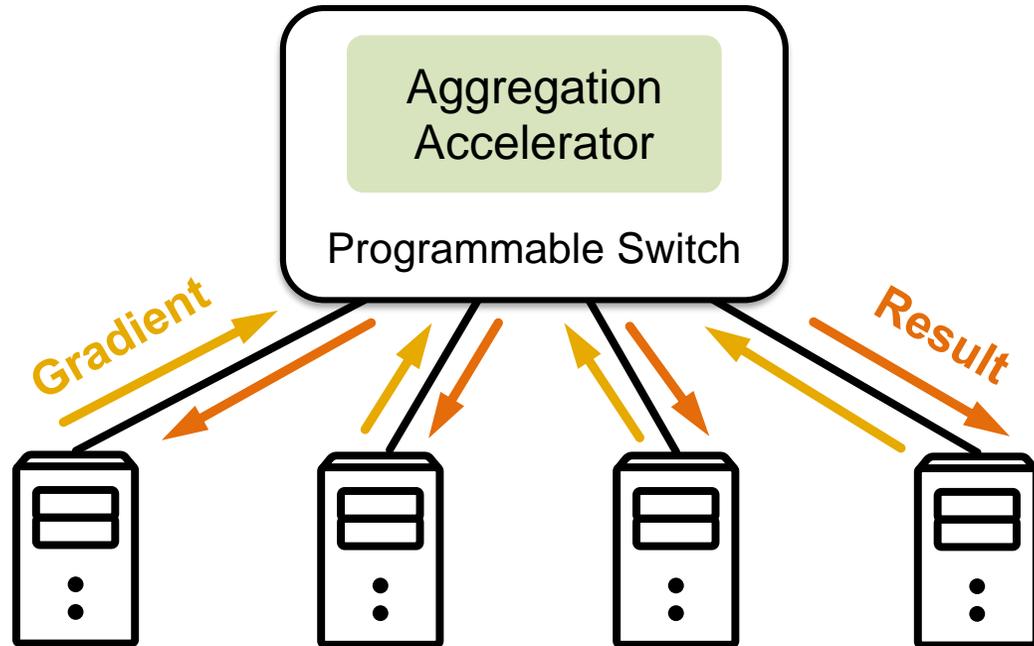
Supporting Different (Sync & Async) Training Execution Modes

Synchronous Distributed Training



Supporting Different (Sync & Async) Training Execution Modes

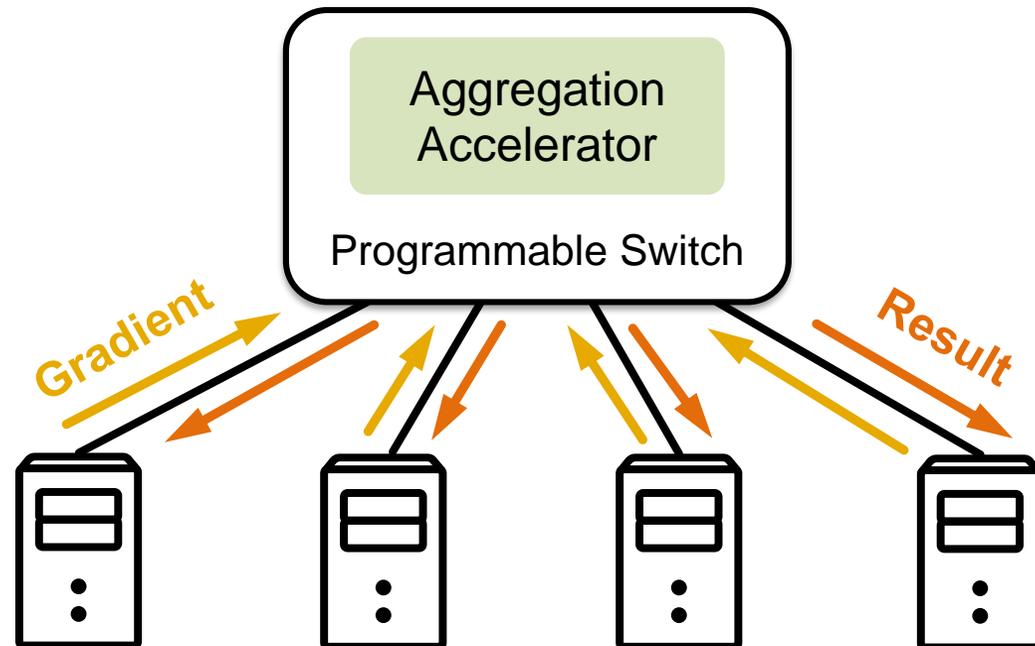
Synchronous Distributed Training



In-Switch Acceleration Directly Applies

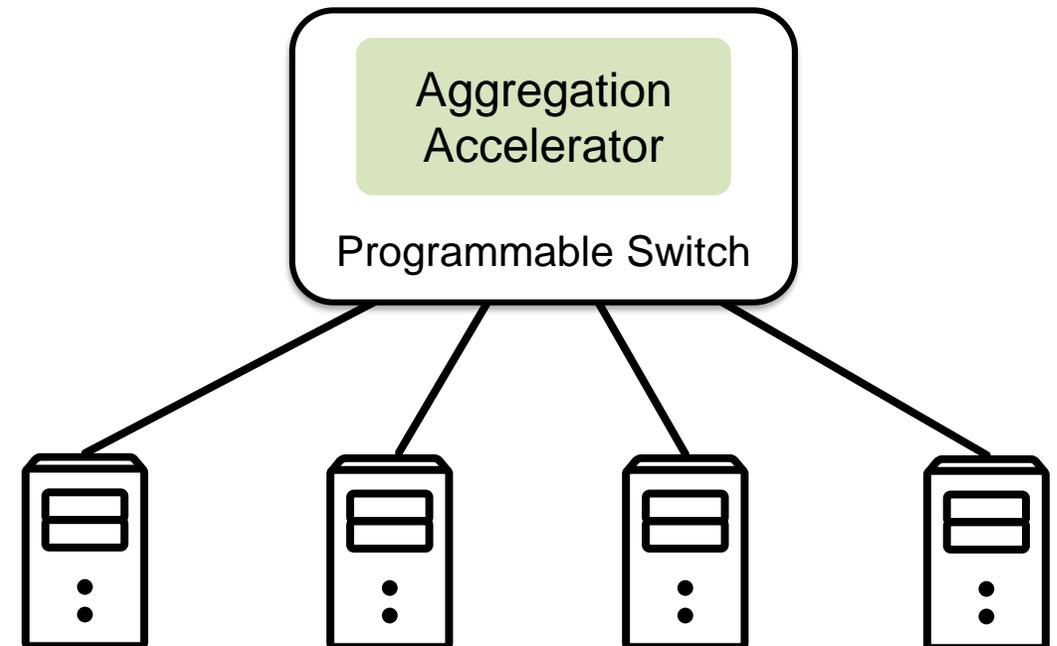
Supporting Different (Sync & Async) Training Execution Modes

Synchronous Distributed Training



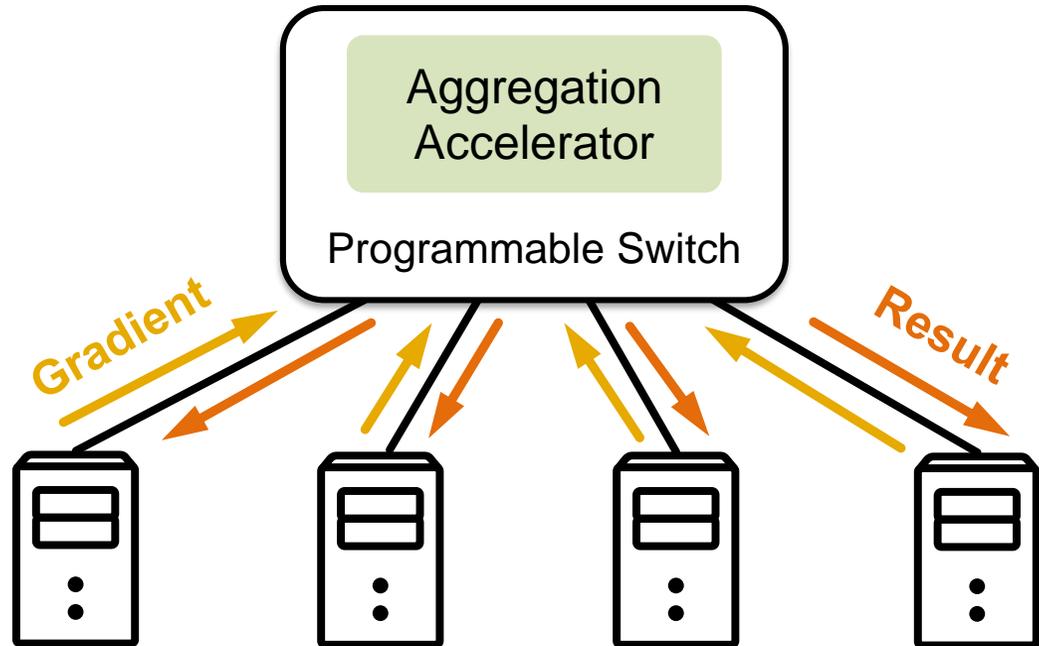
In-Switch Acceleration Directly Applies

Asynchronous Distributed Training



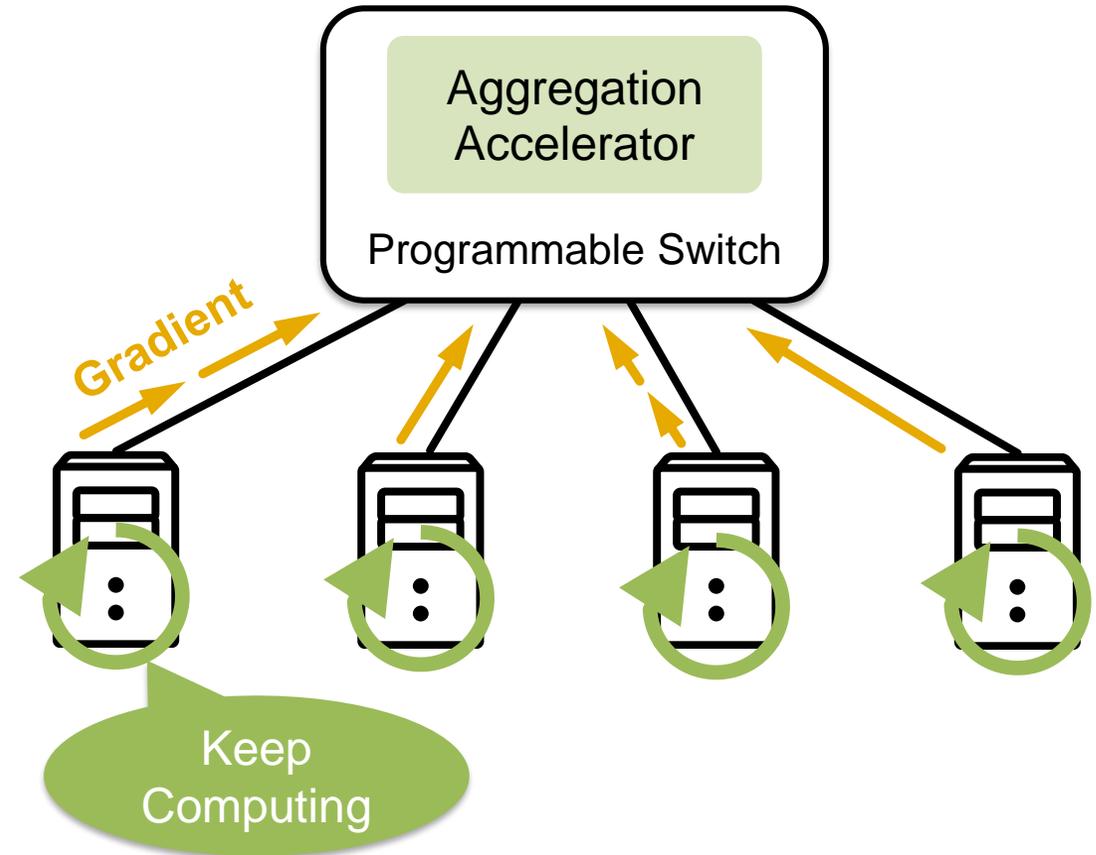
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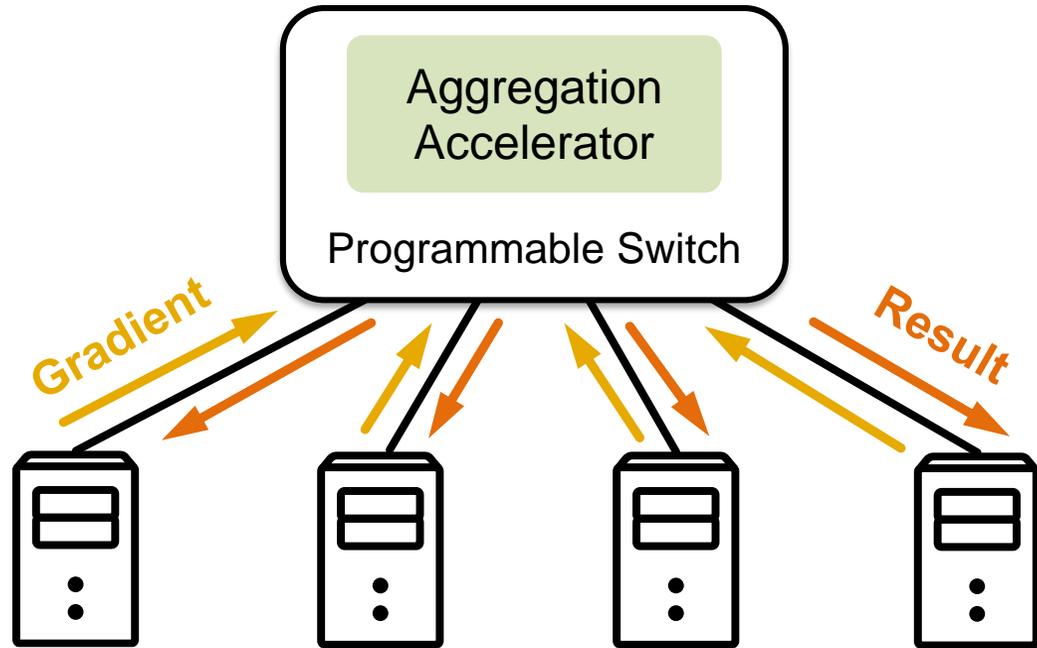
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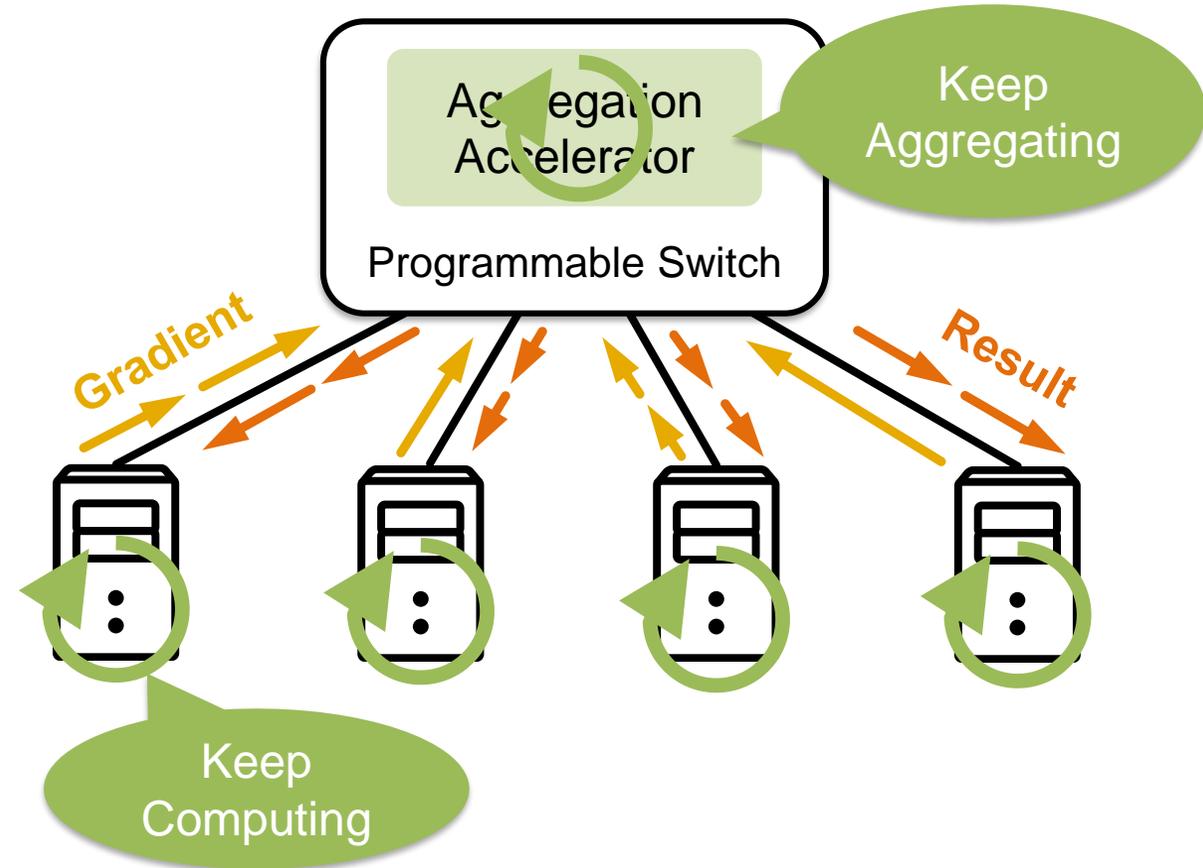
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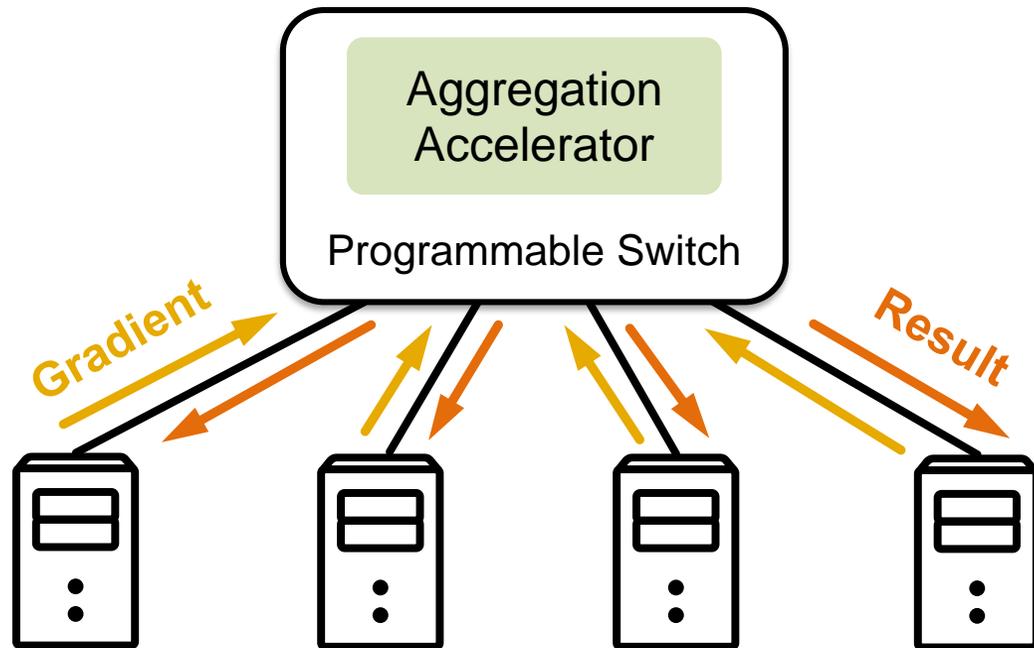
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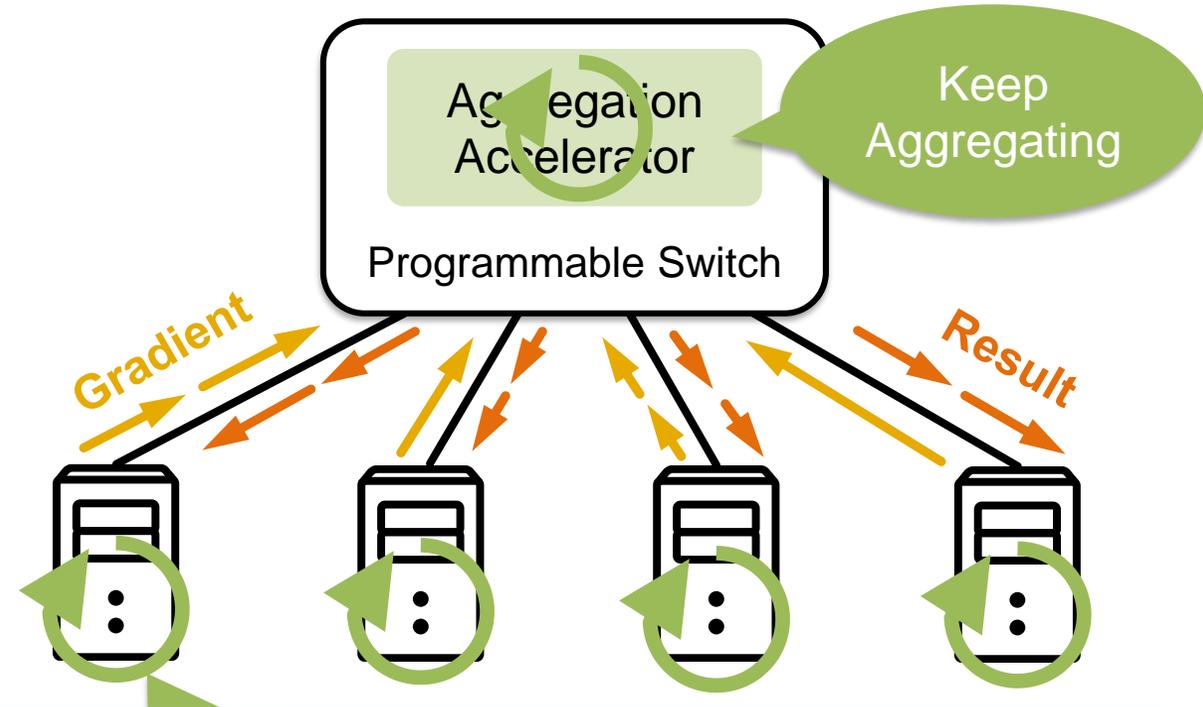
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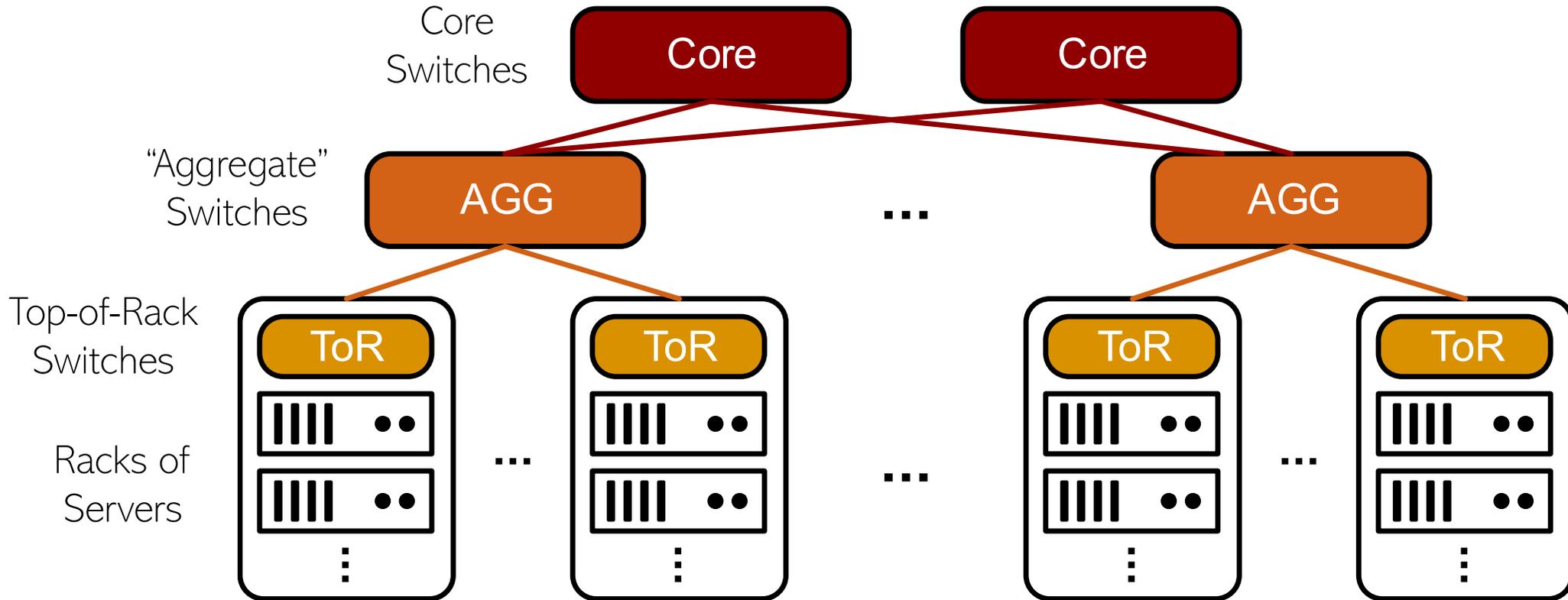
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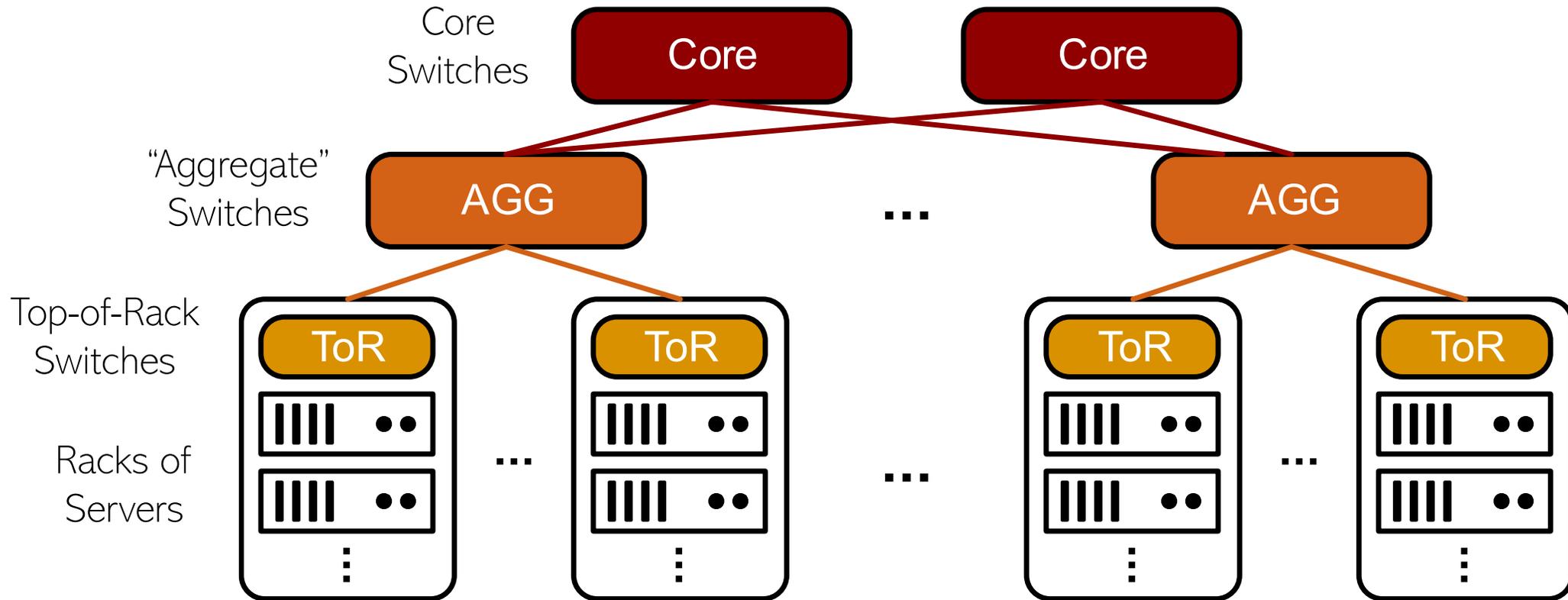
HW/Algo Co-Design For Improved Parallelism

Scaling In-Switch Computing in Rack-Scale Data Centers



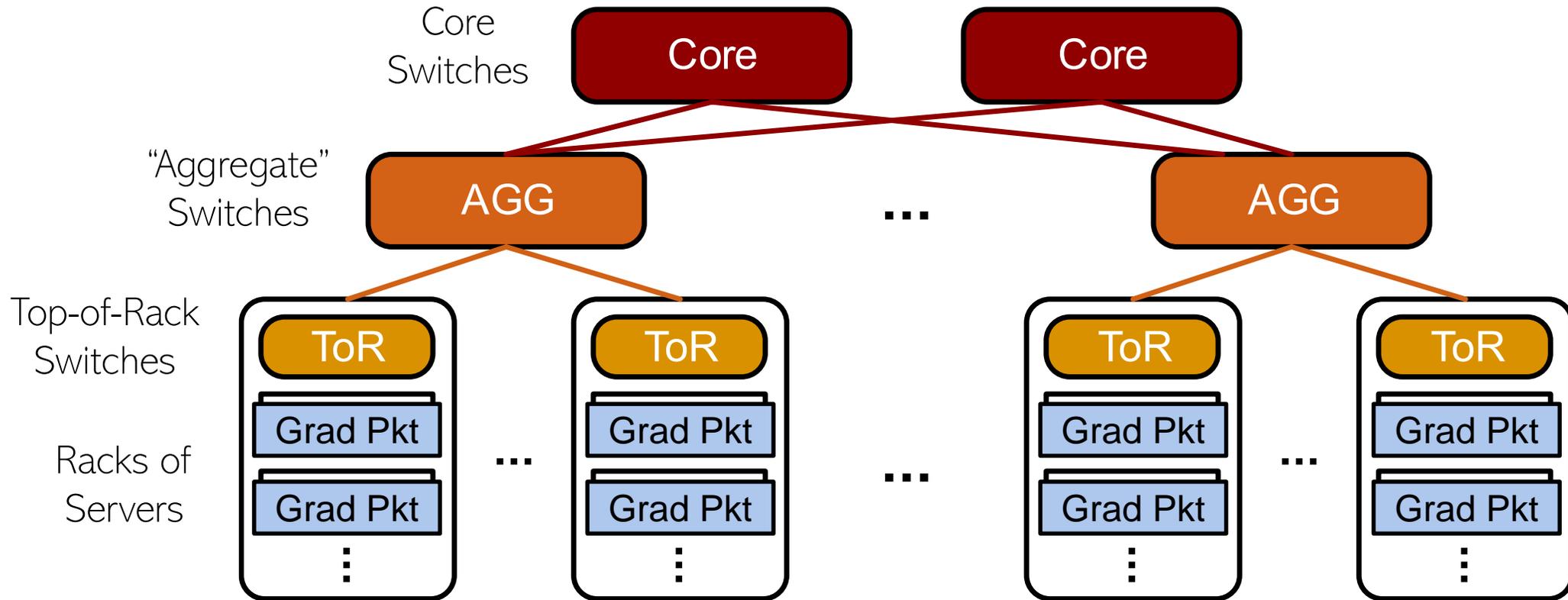
The Typical Network Architecture at Data Center

Scaling In-Switch Computing in Rack-Scale Data Centers



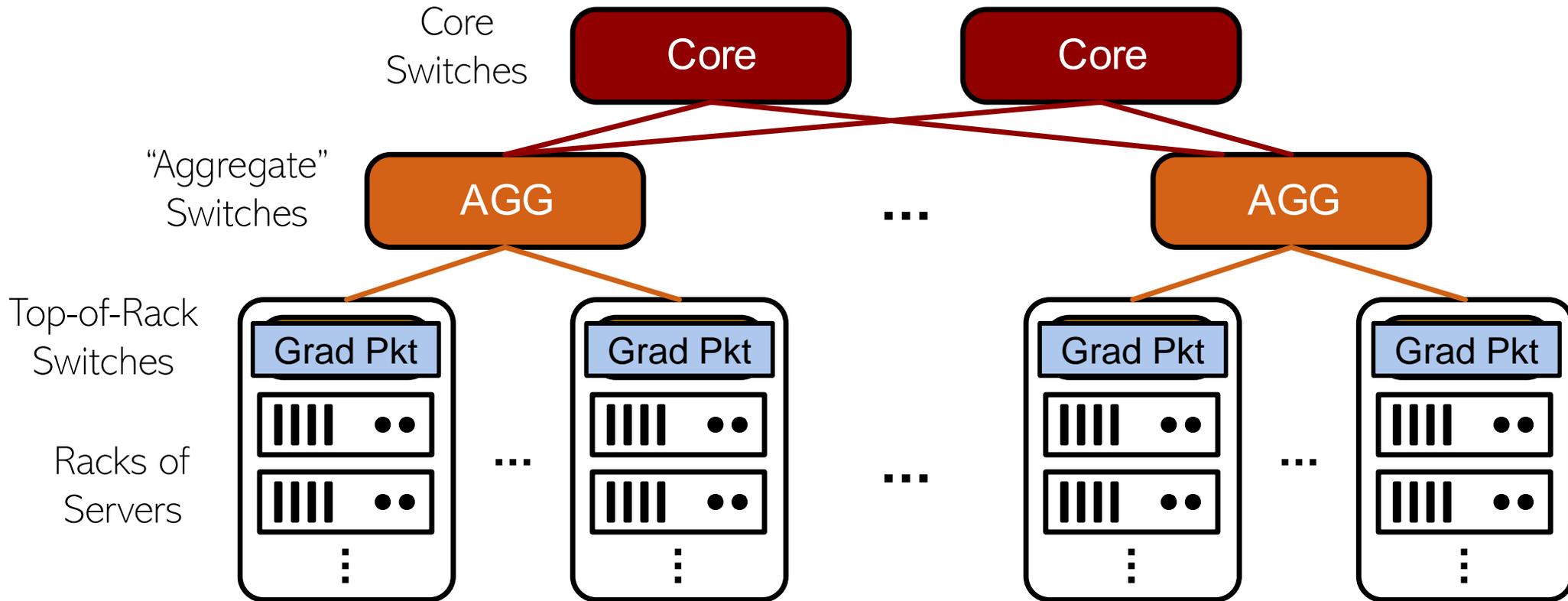
The Hierarchical Aggregation of iSwitch

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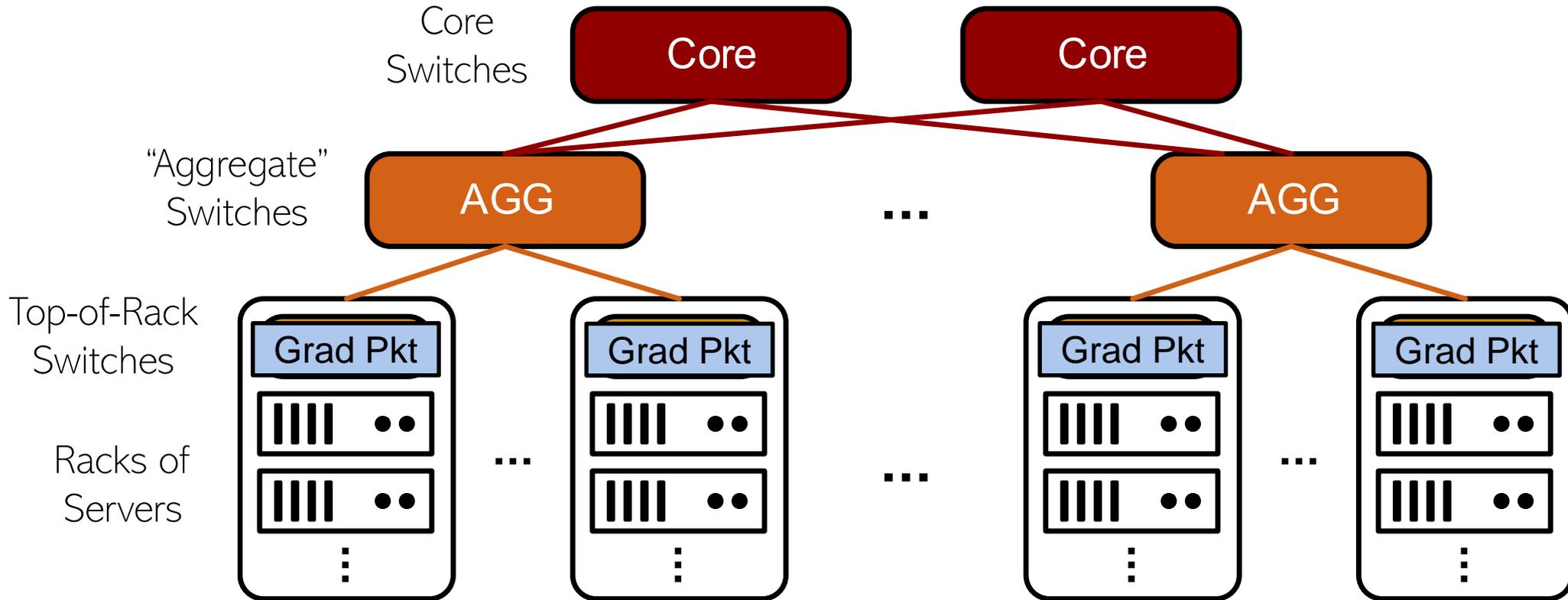
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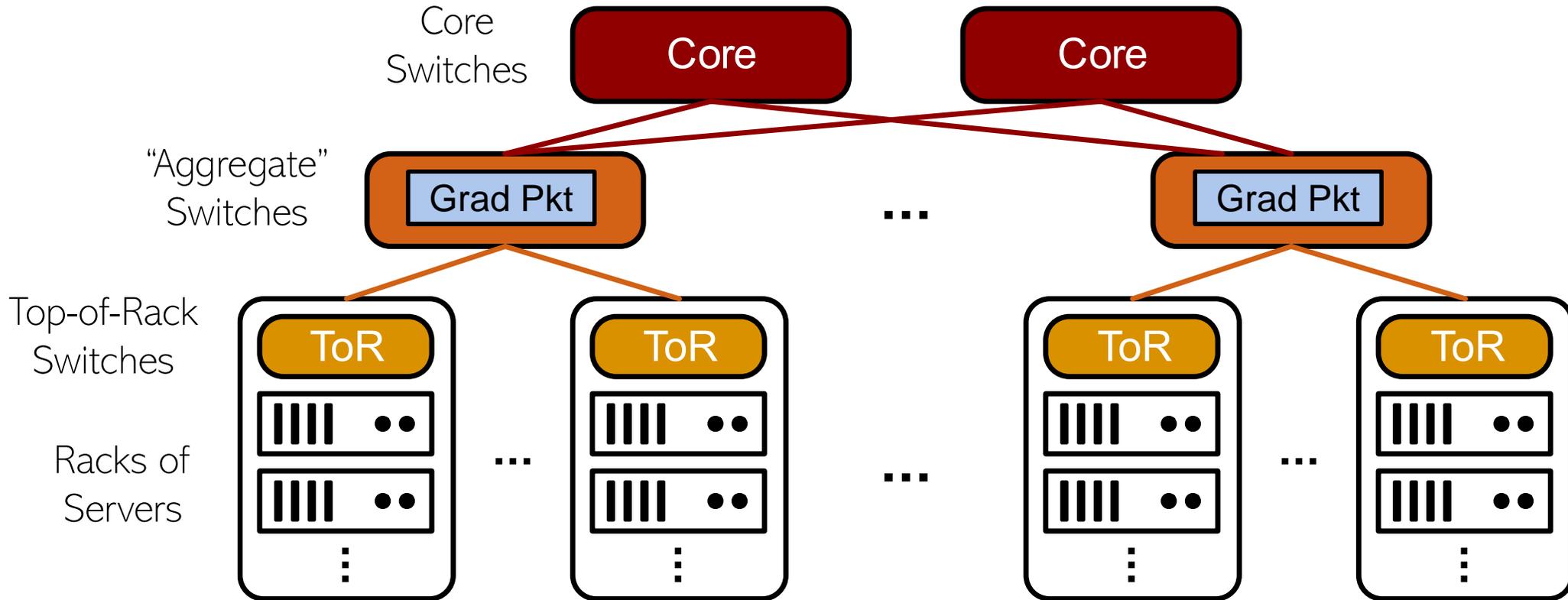
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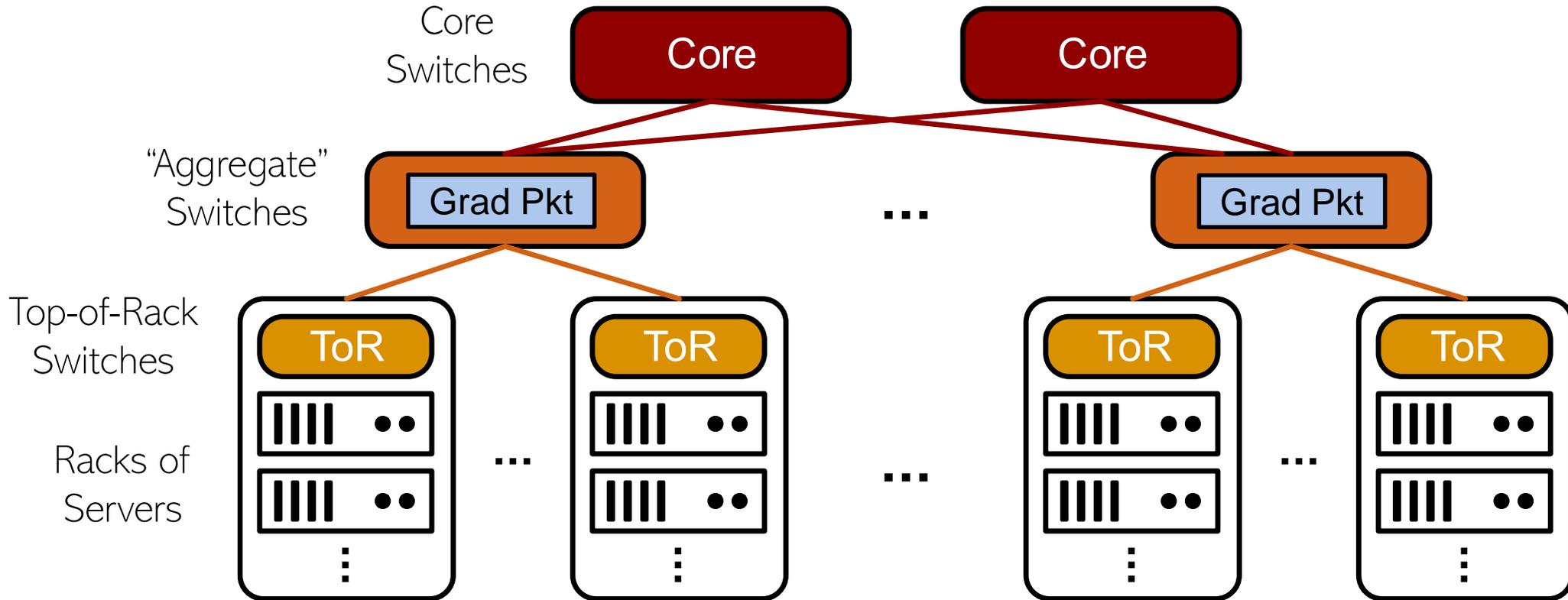
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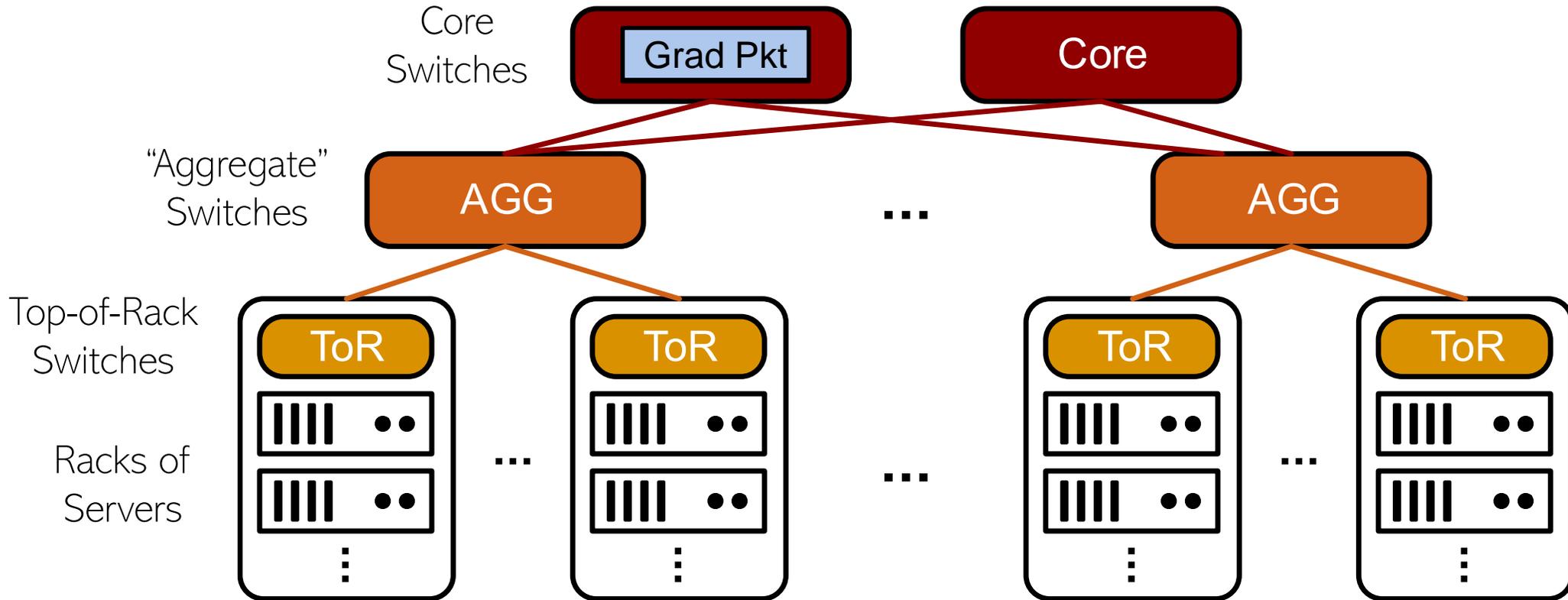
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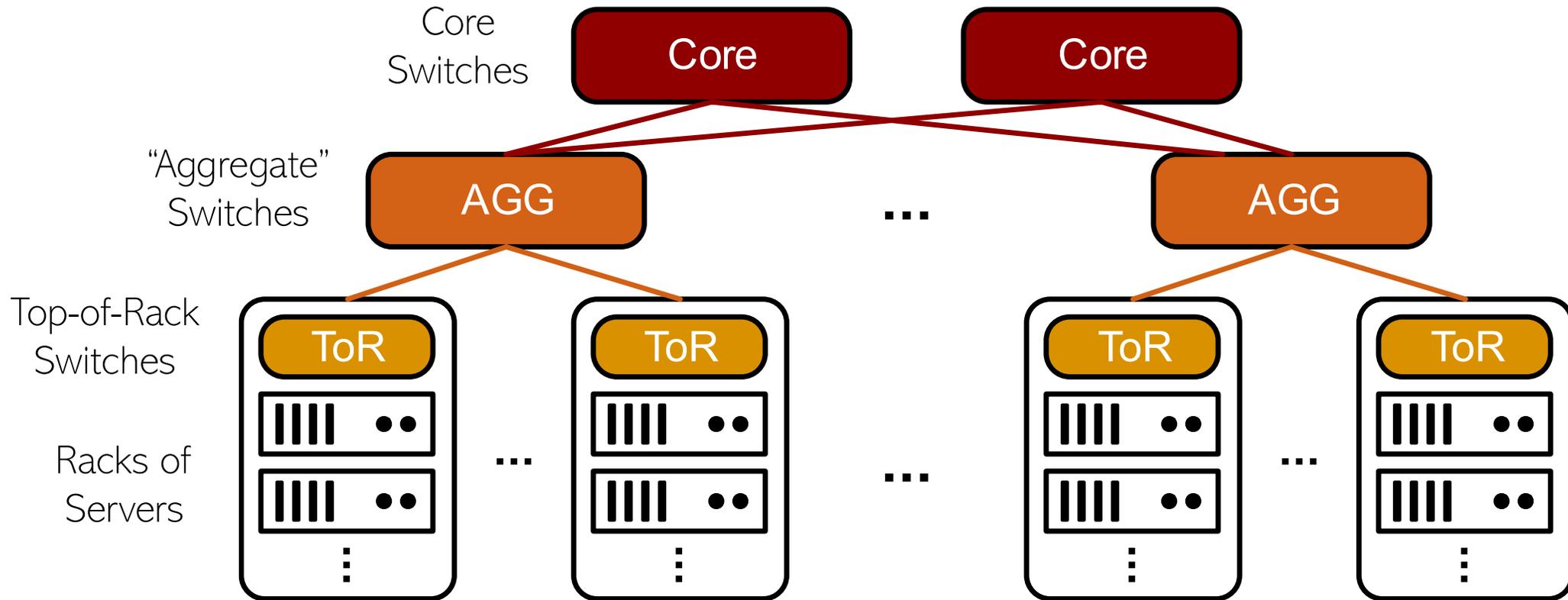
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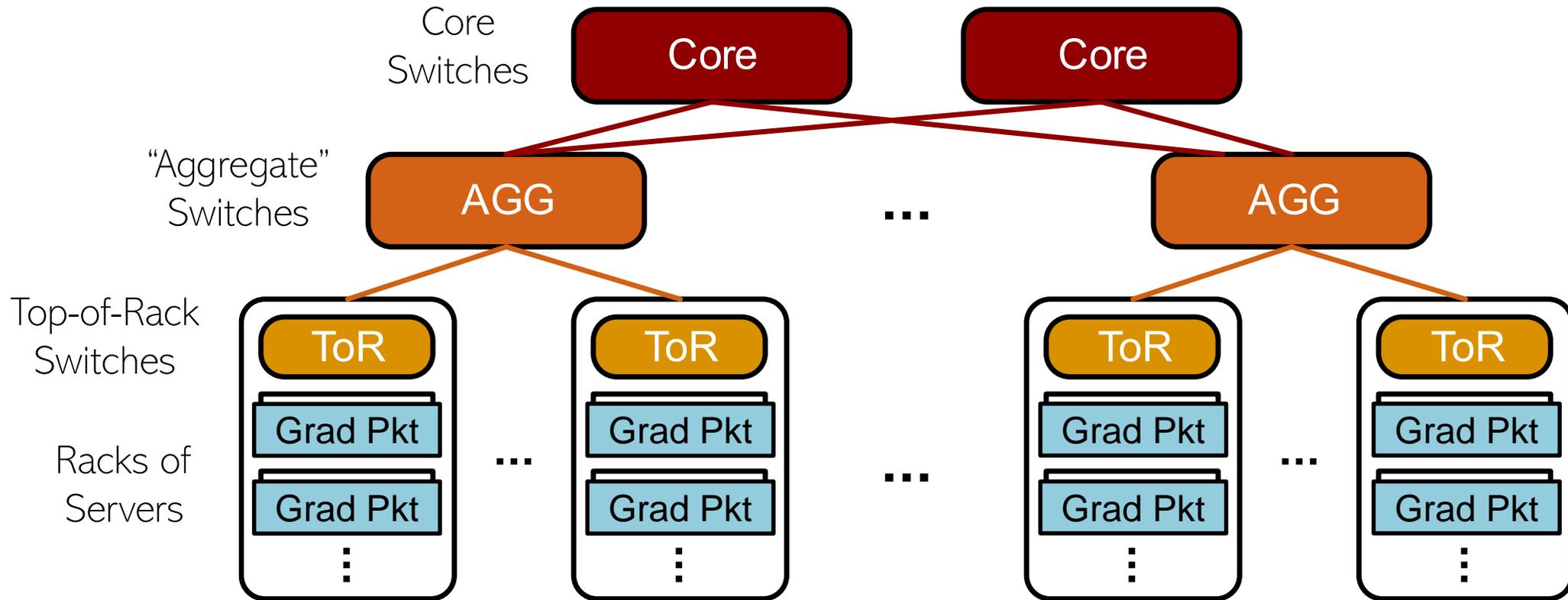
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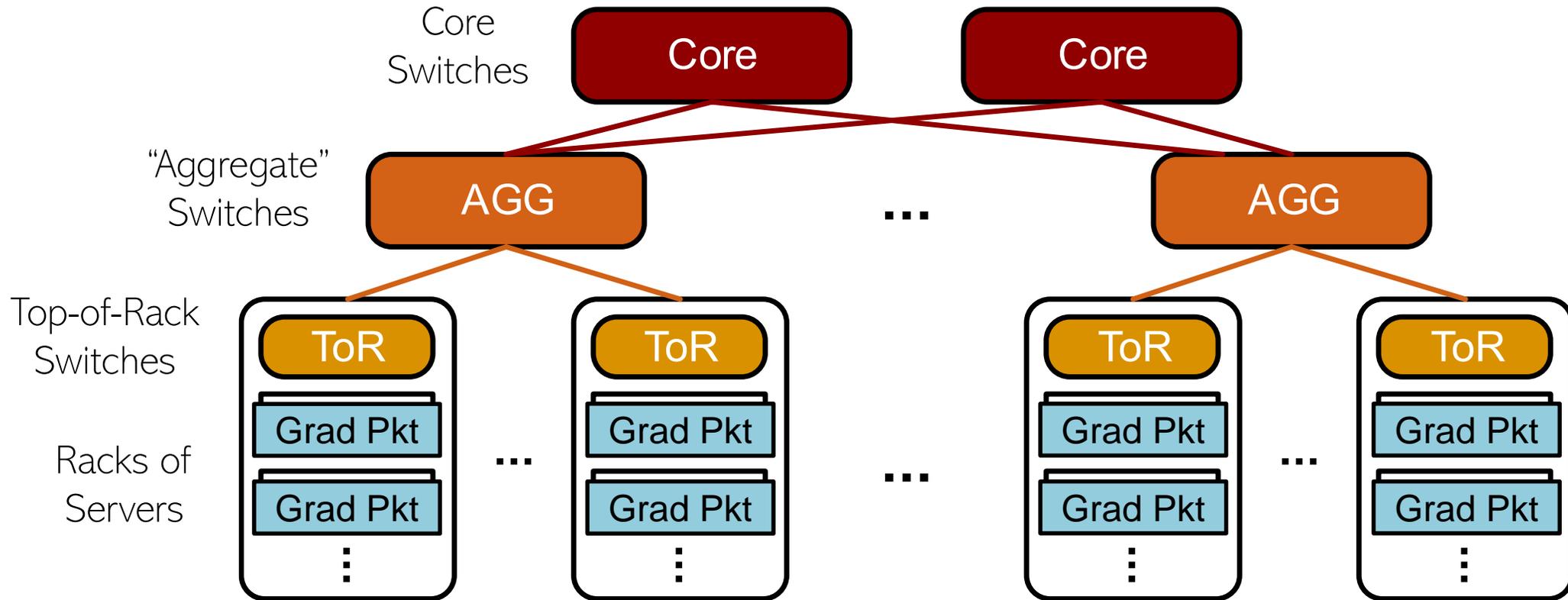
The Hierarchical Aggregation of iSwitch

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The Hierarchical Aggregation of iSwitch

Scaling In-Switch Computing in Rack-Scale Data Centers



No Additional Cost or Topology Change for Scaling In-Switch Computing

In-Switch Computing Implementation



NetFPGA-SUME Board



GPU Cluster

RL Training Benchmarks

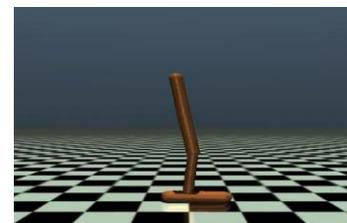
DQN



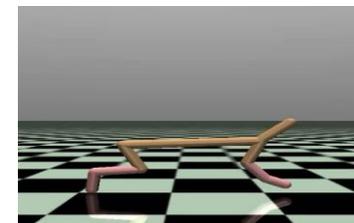
A2C



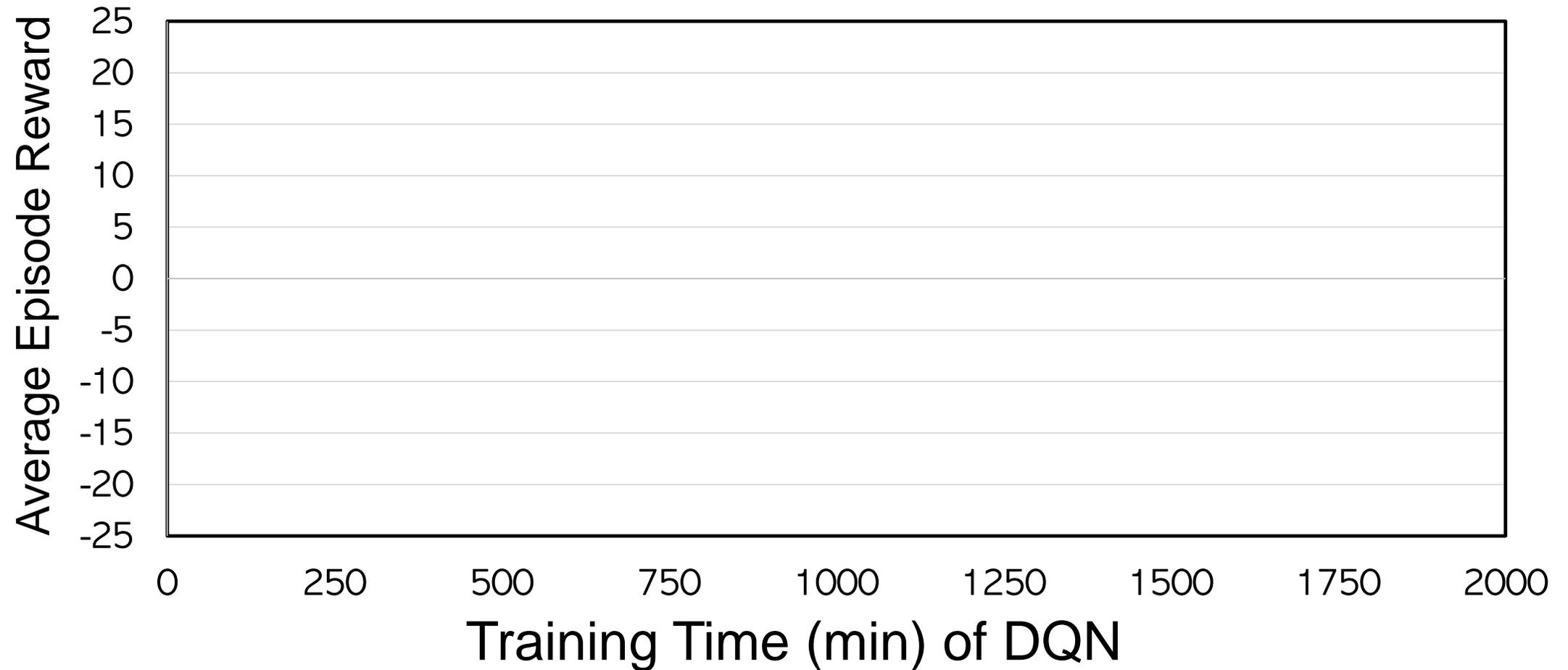
PPO



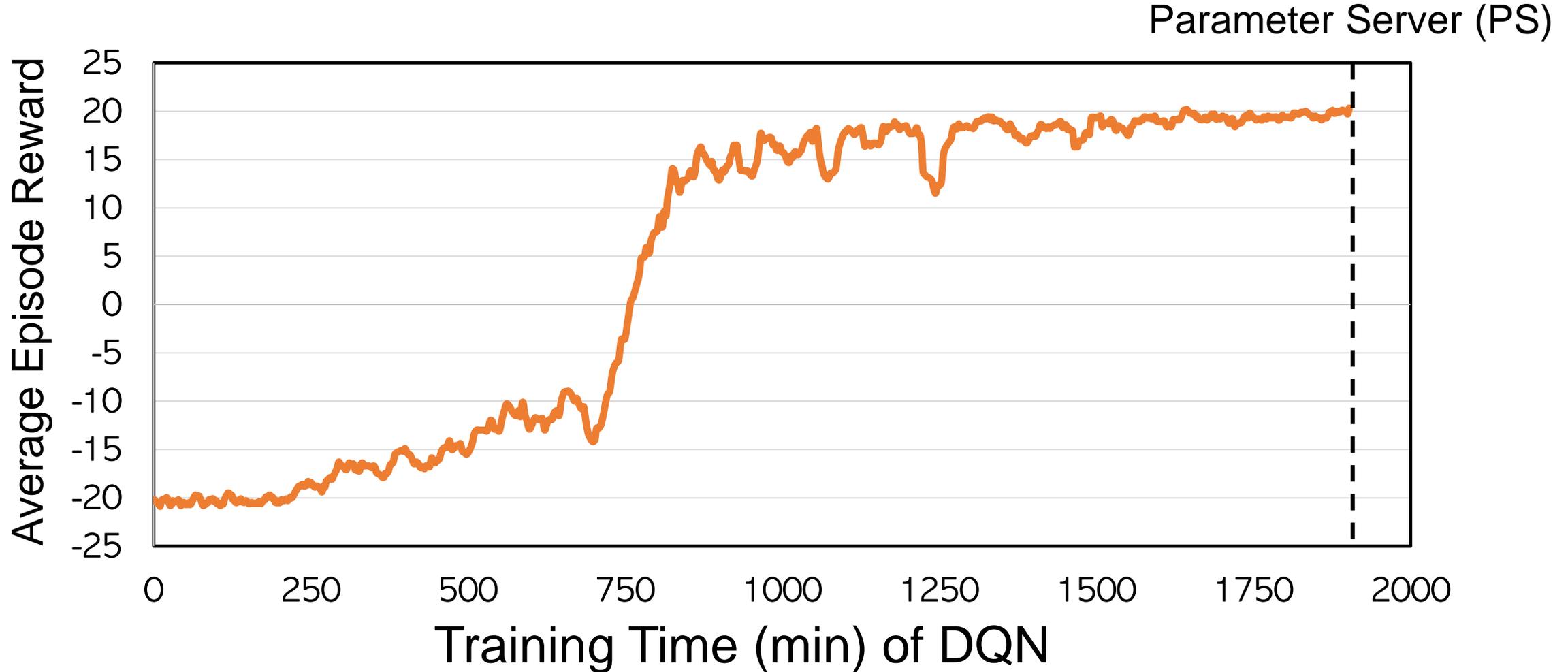
DDPG



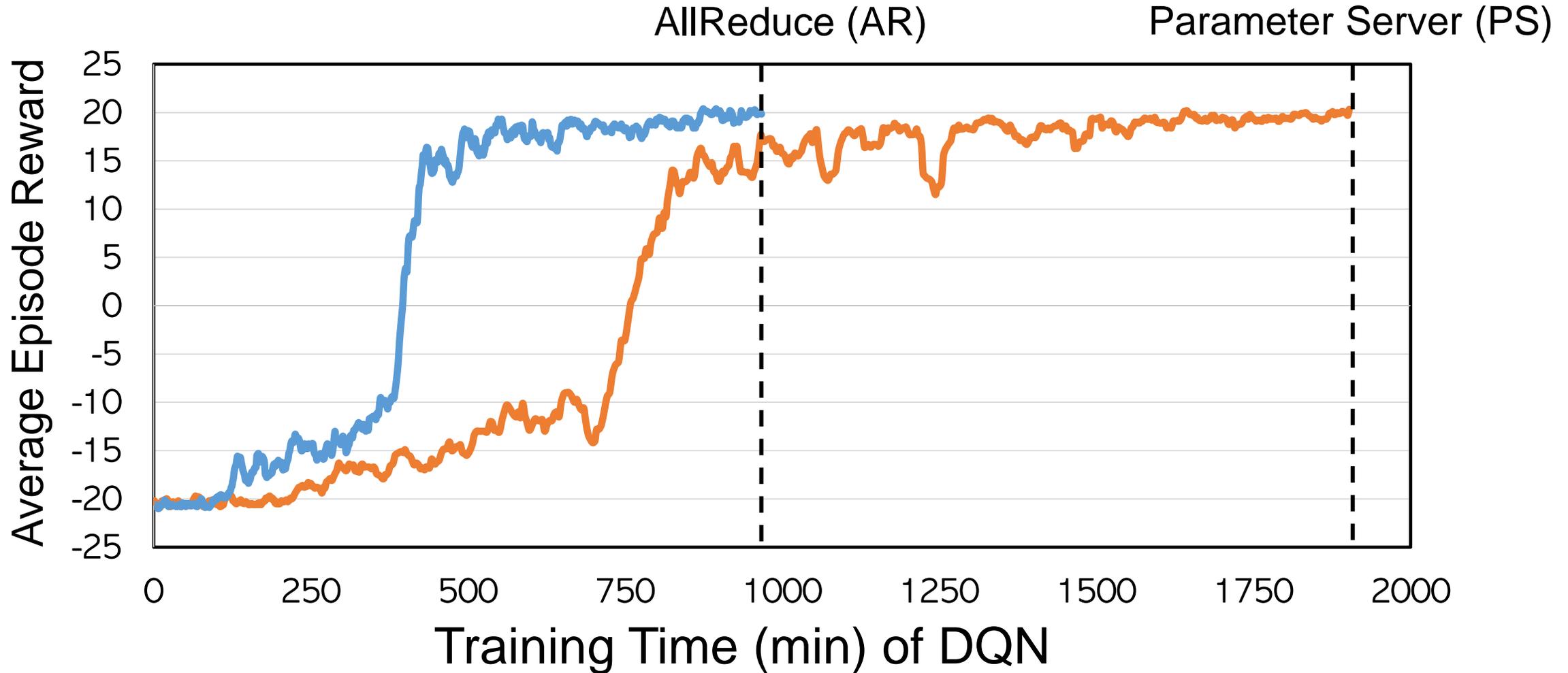
Reducing the End-to-End Training Time with iSwitch



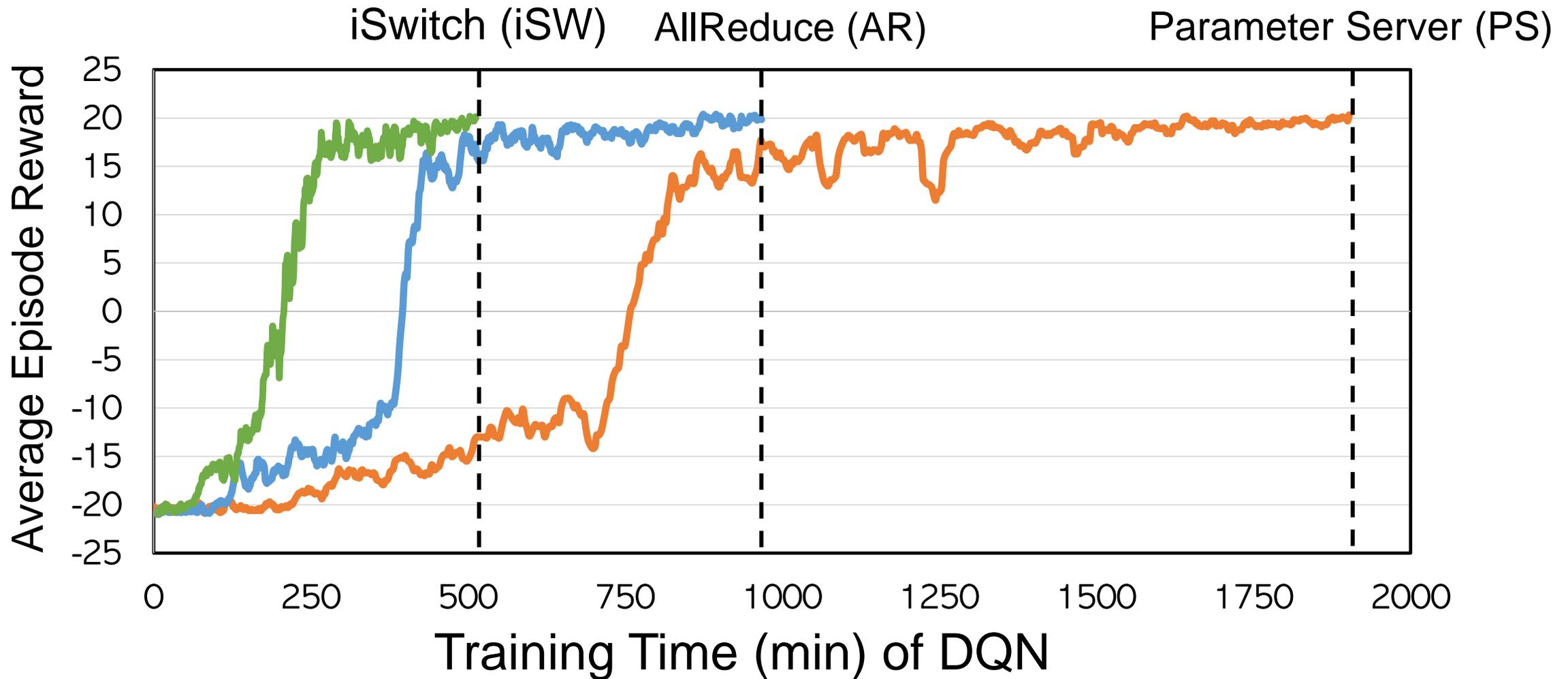
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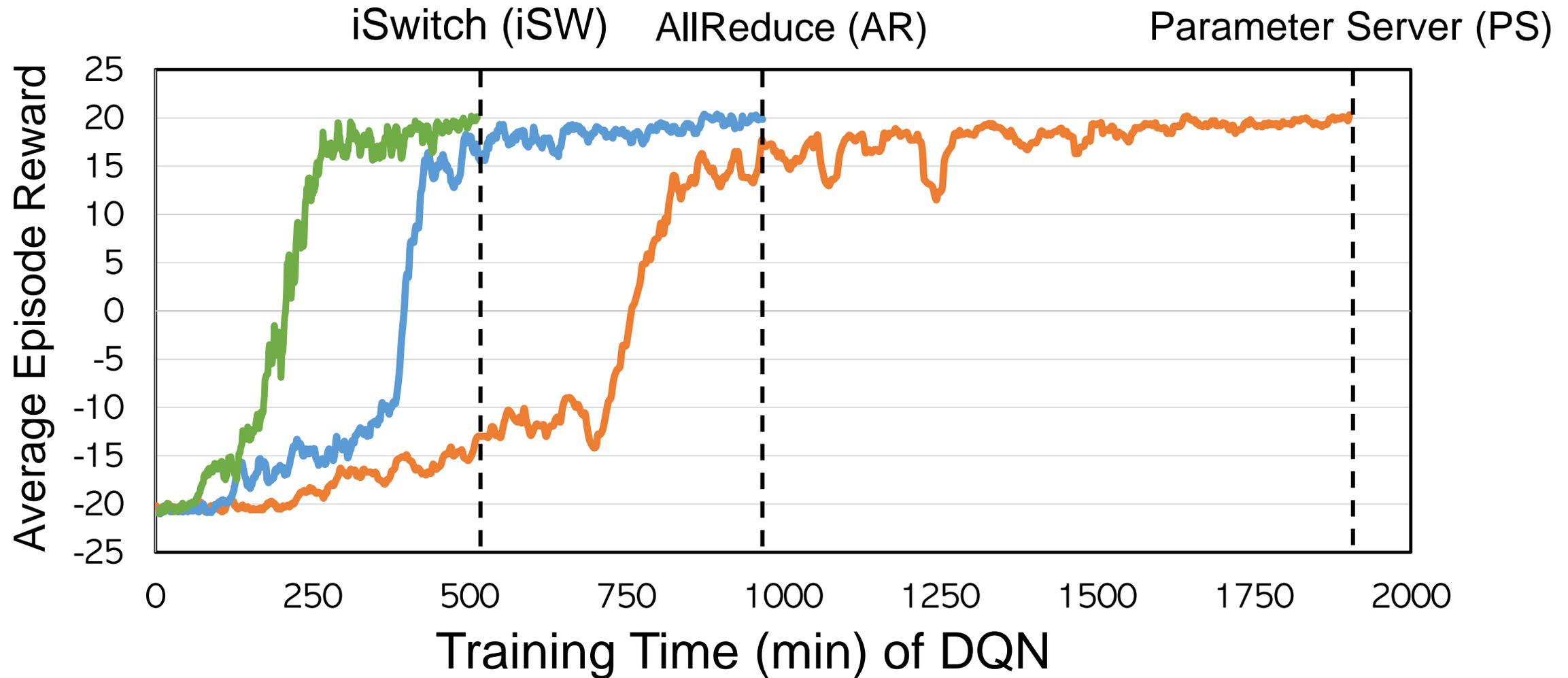
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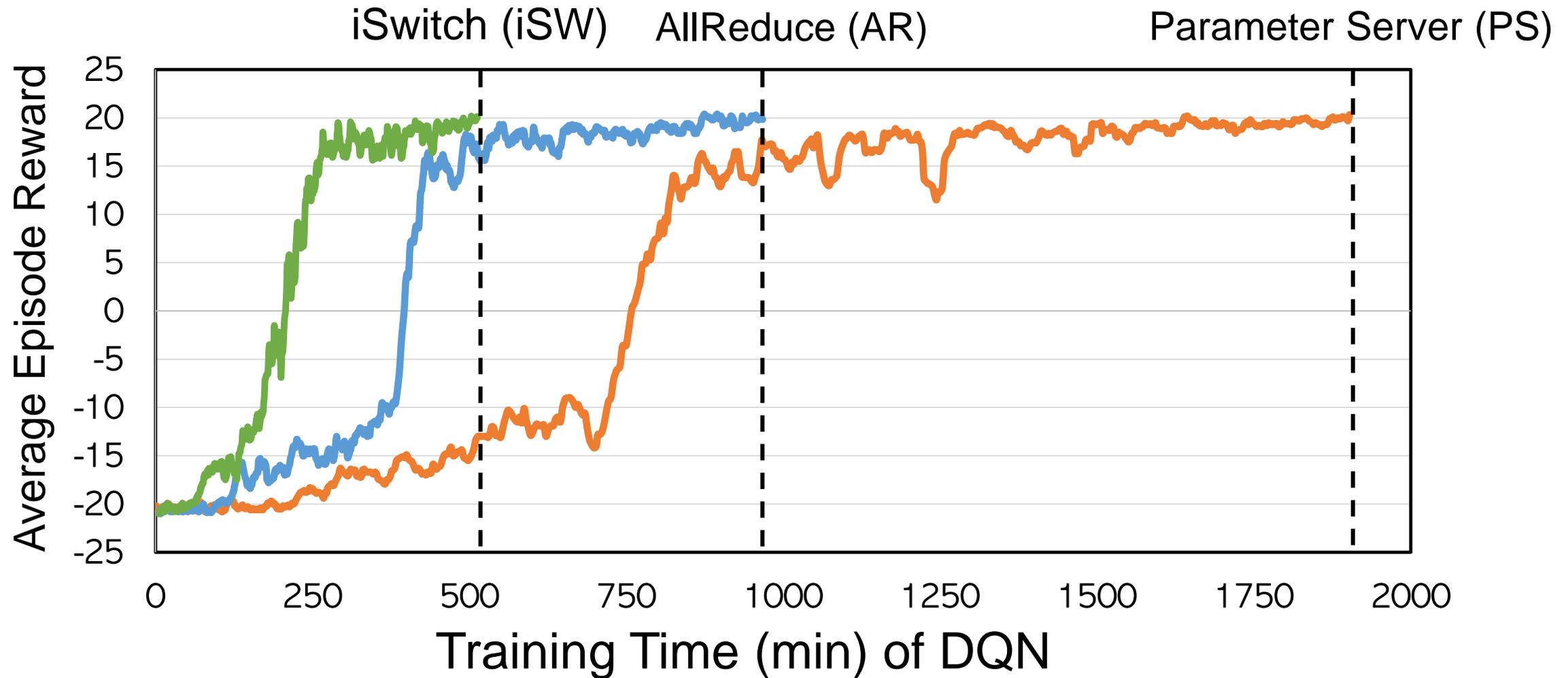
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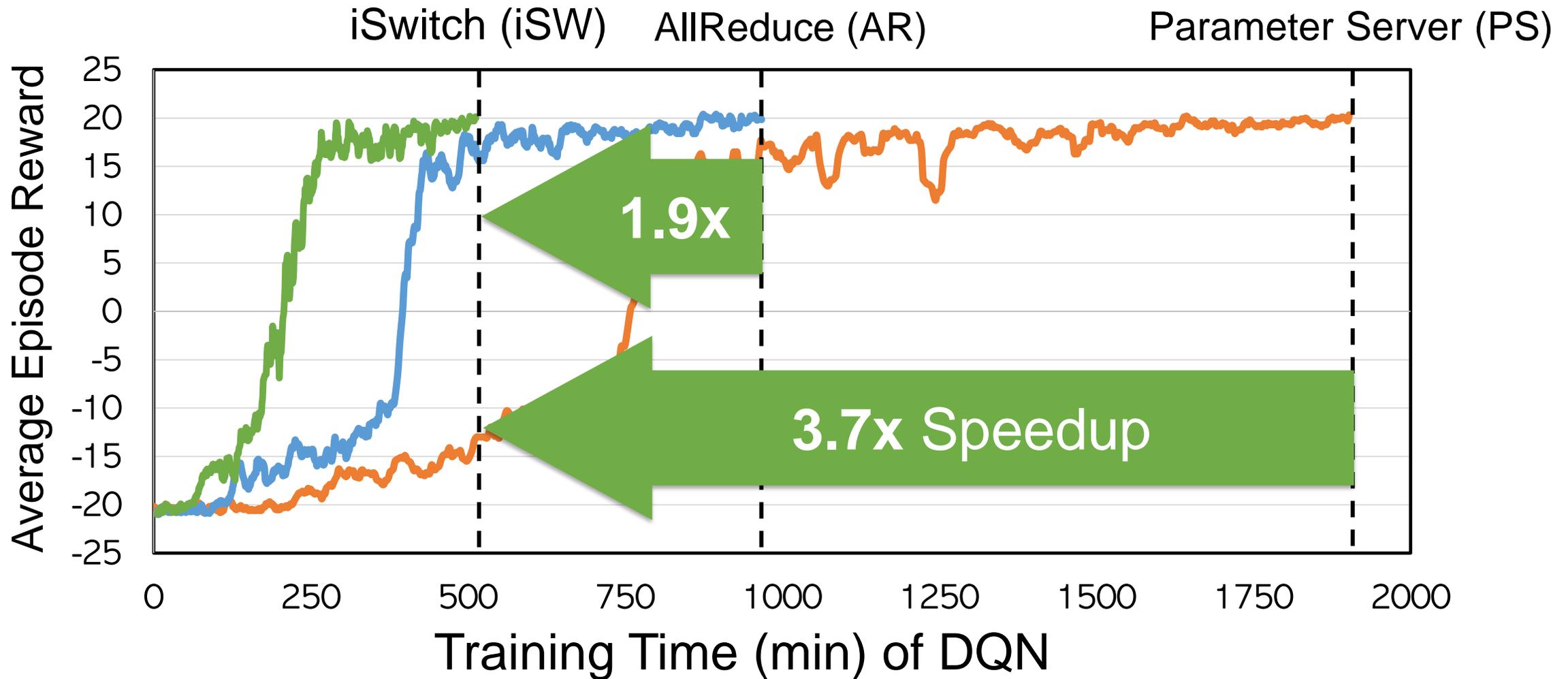
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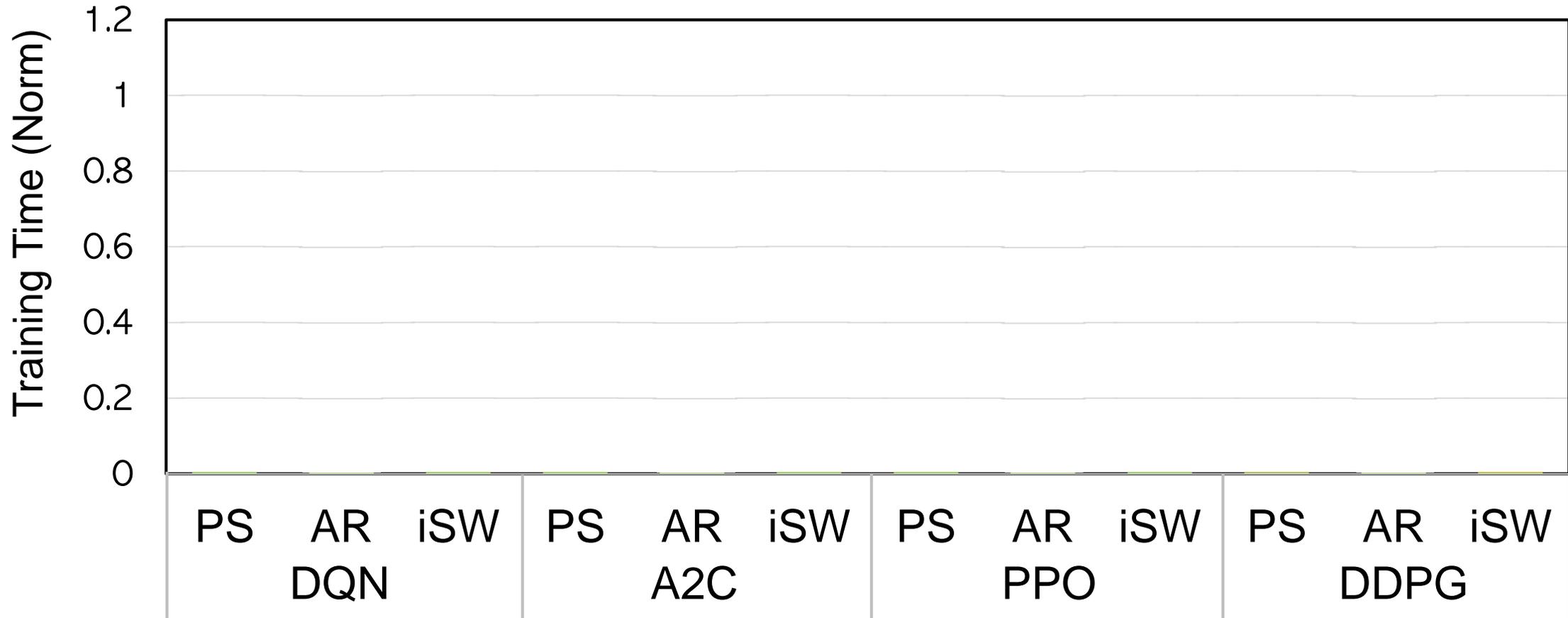


Reducing the End-to-End Training Time with iSwitch



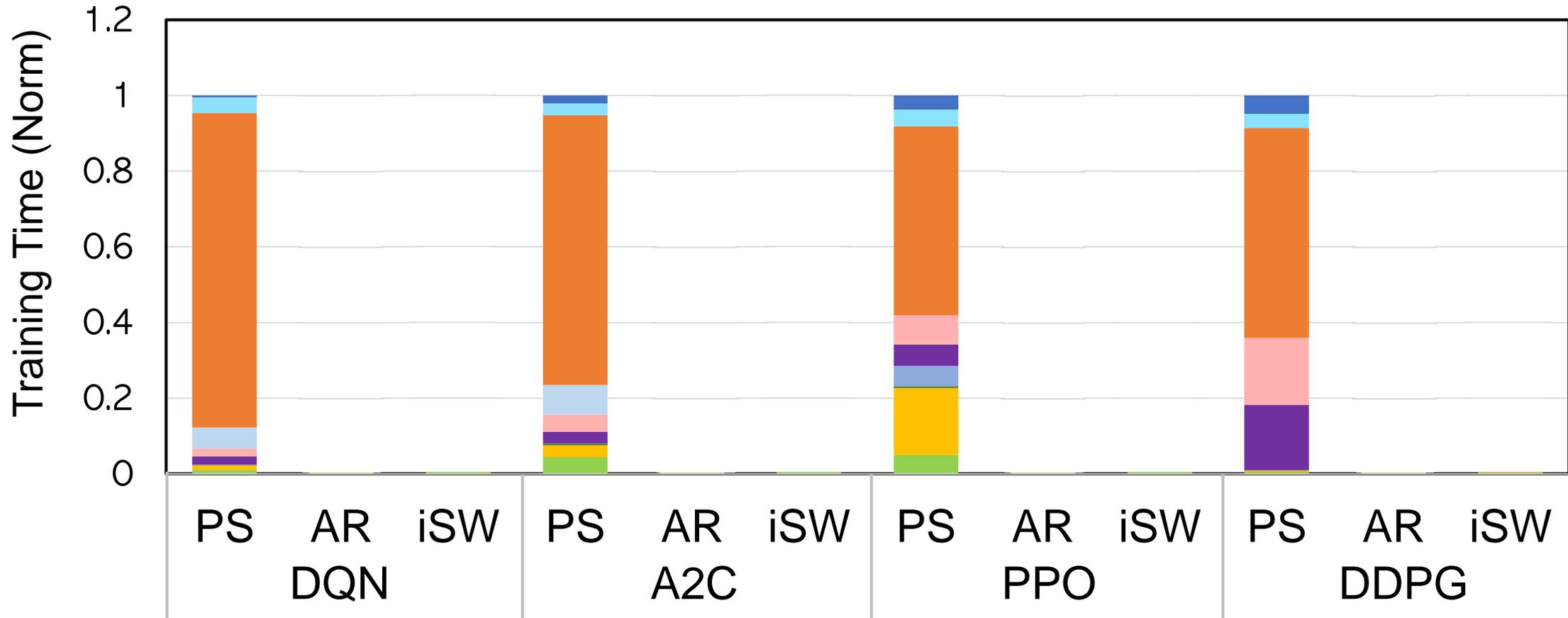
Performance Breakdown for Each Training Iteration

- Agent Action
- Environment
- Buffer Sampling
- Memory Alloc
- Forward Pass
- Backward Pass
- GPU Copy
- Grad Aggregation
- Weight Update
- Others



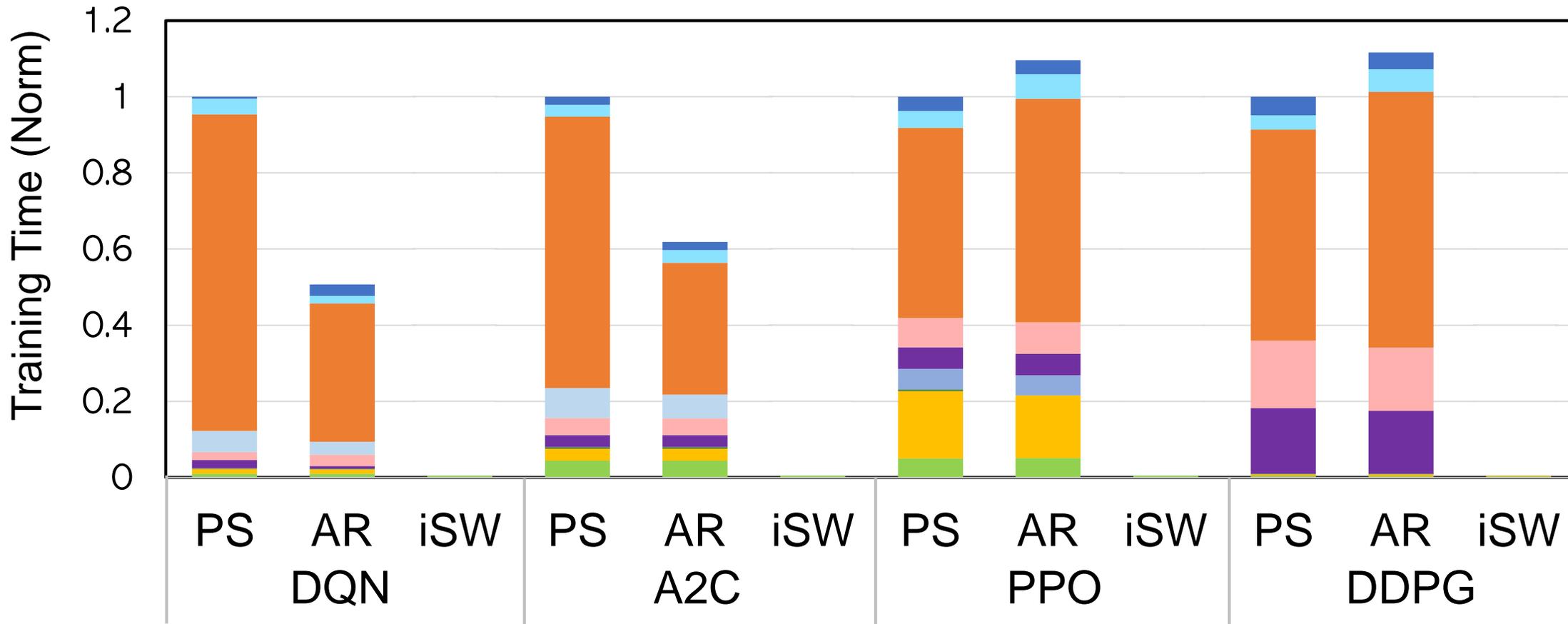
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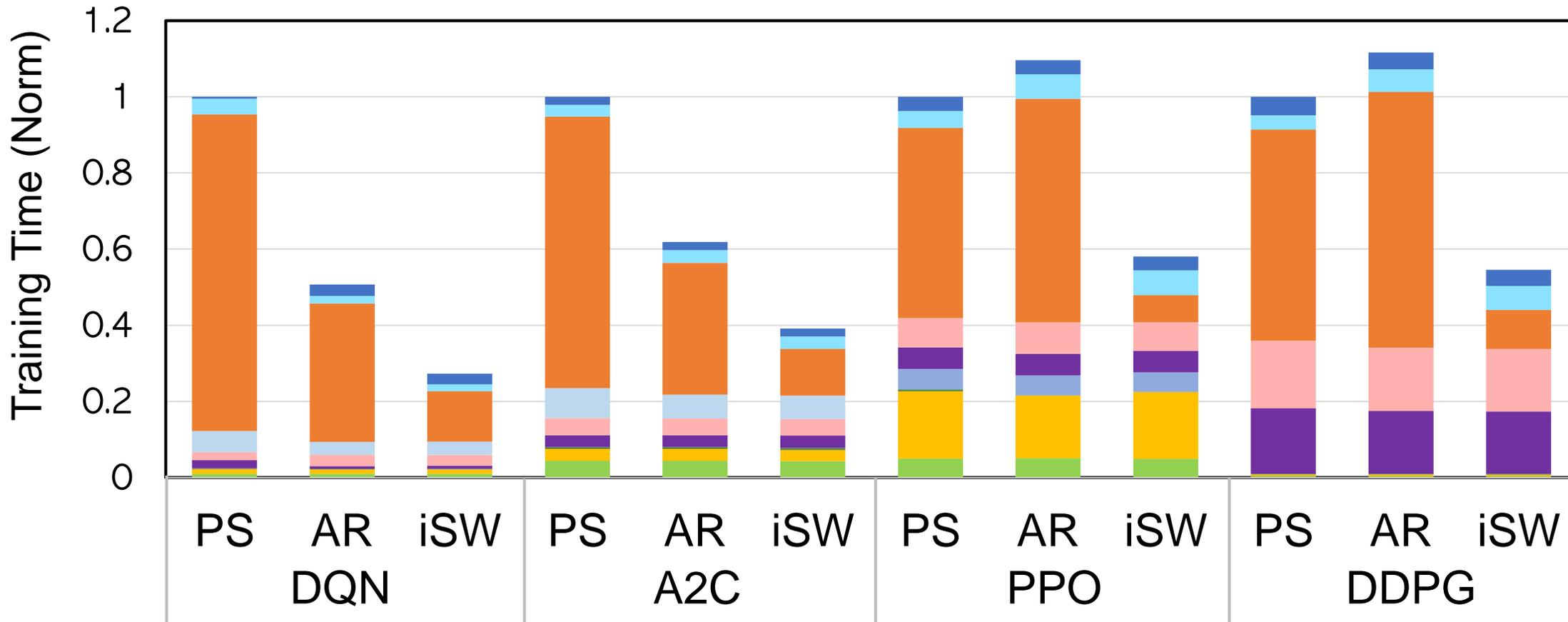
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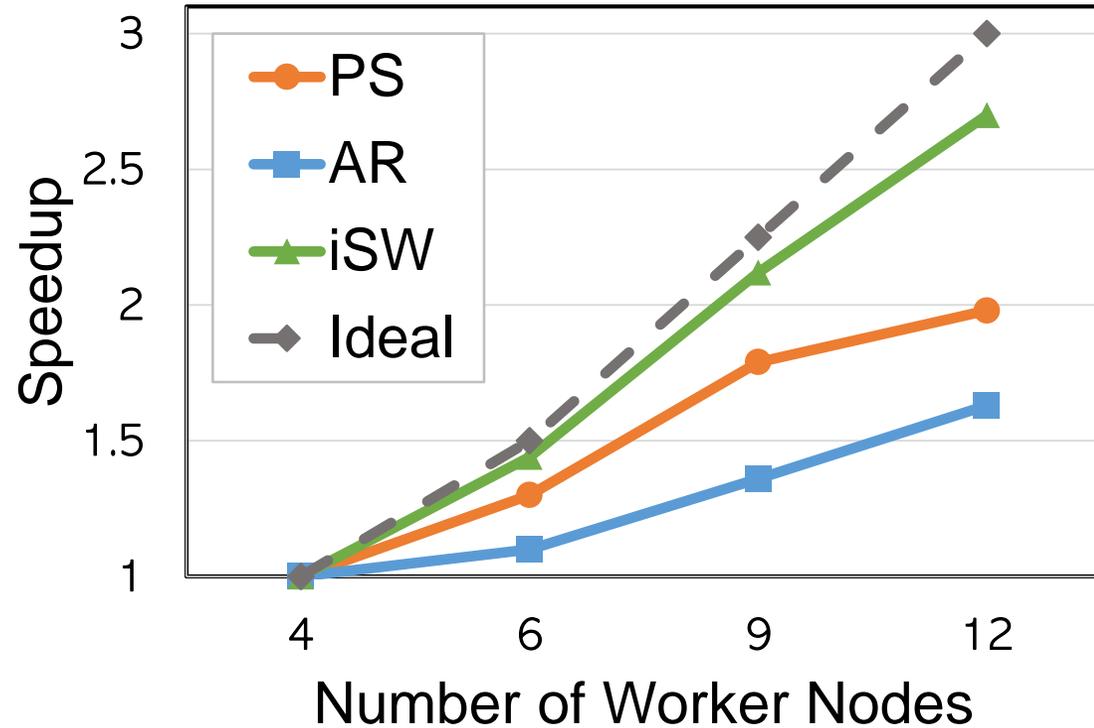
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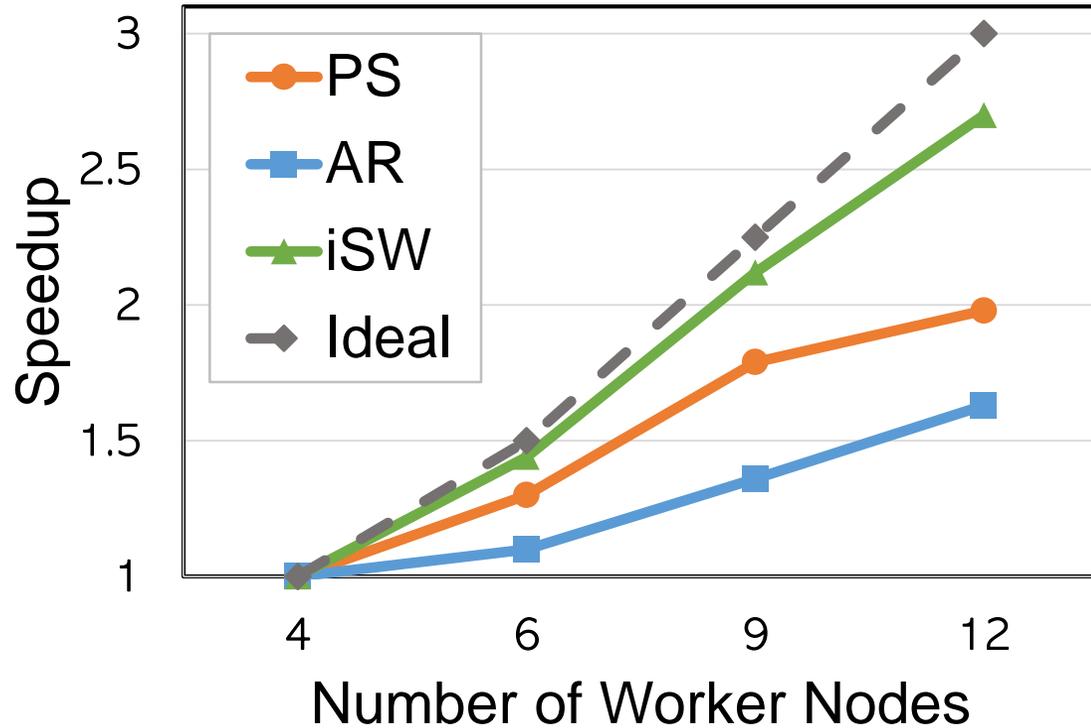
Improved Training Scalability with In-Switch Computing

Synchronous Training of PPO

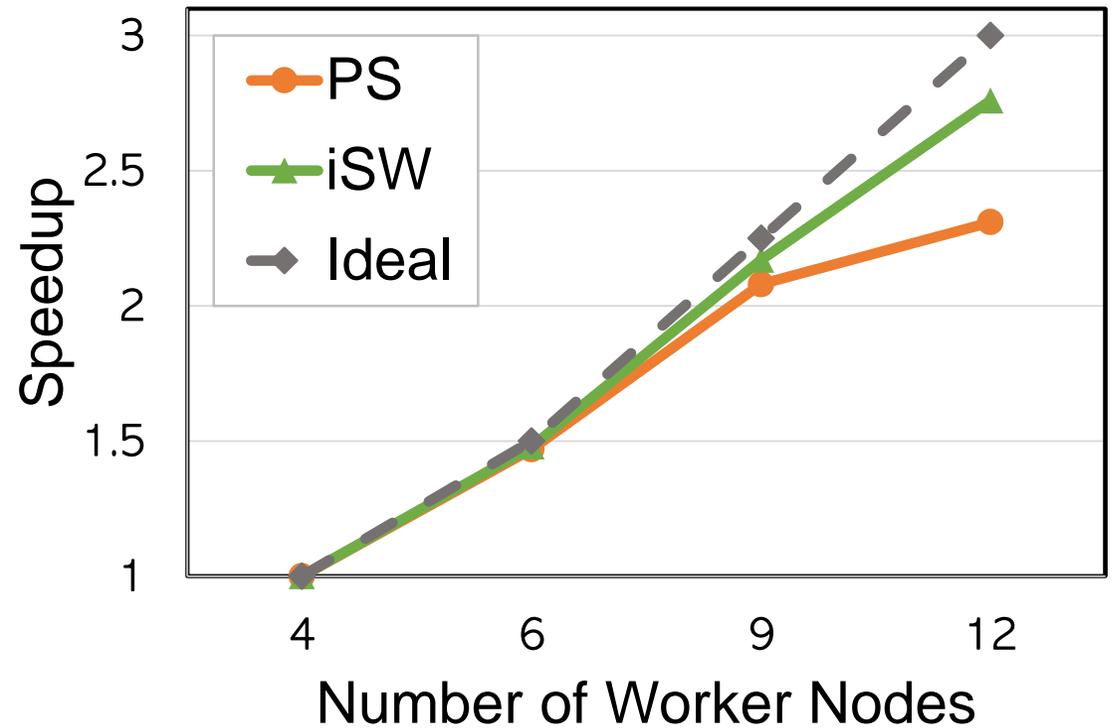


Improved Training Scalability with In-Switch Computing

Synchronous Training of PPO

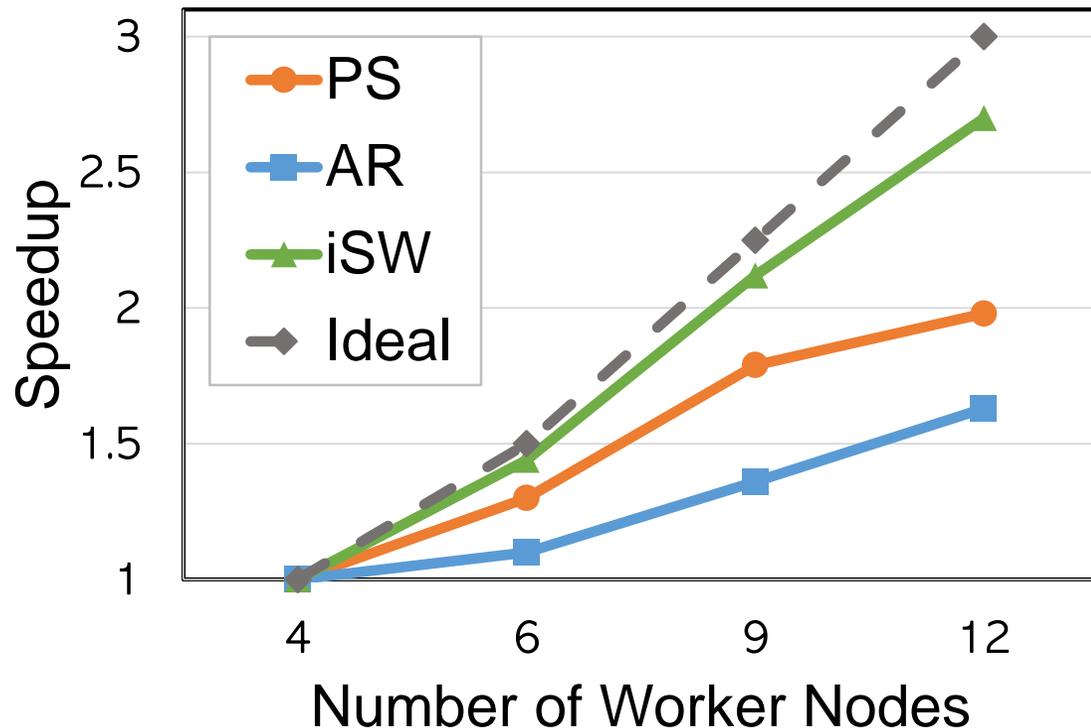


Asynchronous Training of PPO

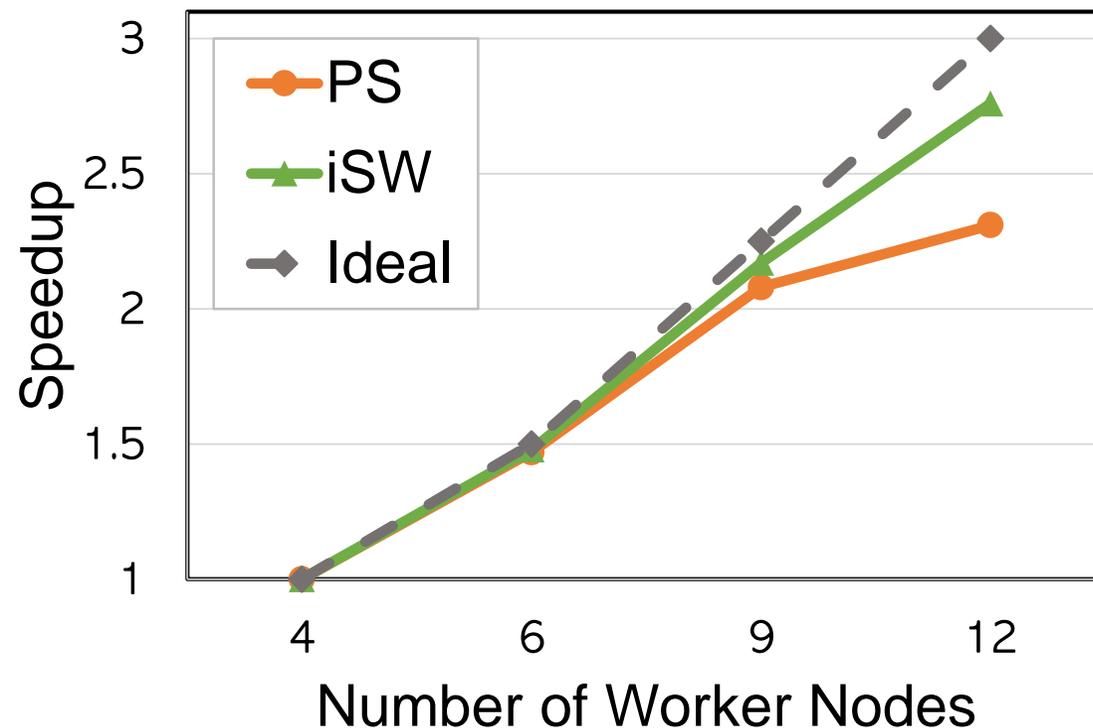


Improved Training Scalability with In-Switch Computing

Synchronous Training of PPO

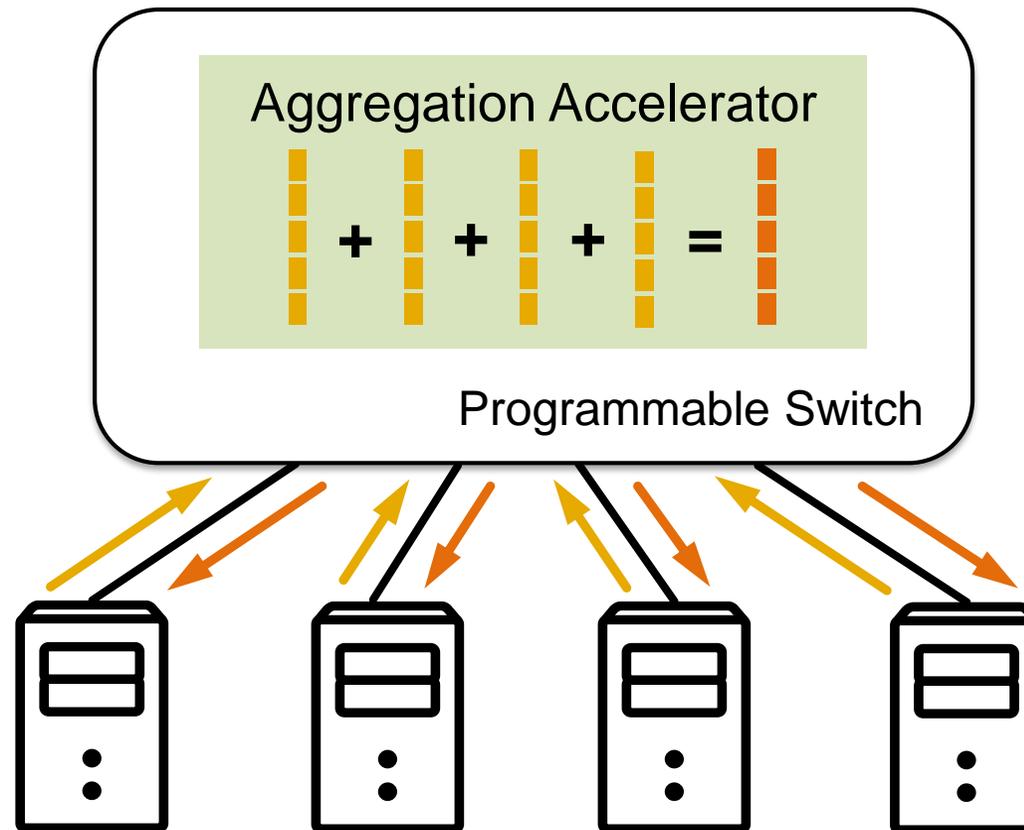


Asynchronous Training of PPO



Close-to Linear Speedup for Both Training Modes

In-Switch Computing Summary



3.7x Speedup for Both Sync/Async Training

Scales at **Rack-Scale** Clusters

Thanks!

Youjie Li

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